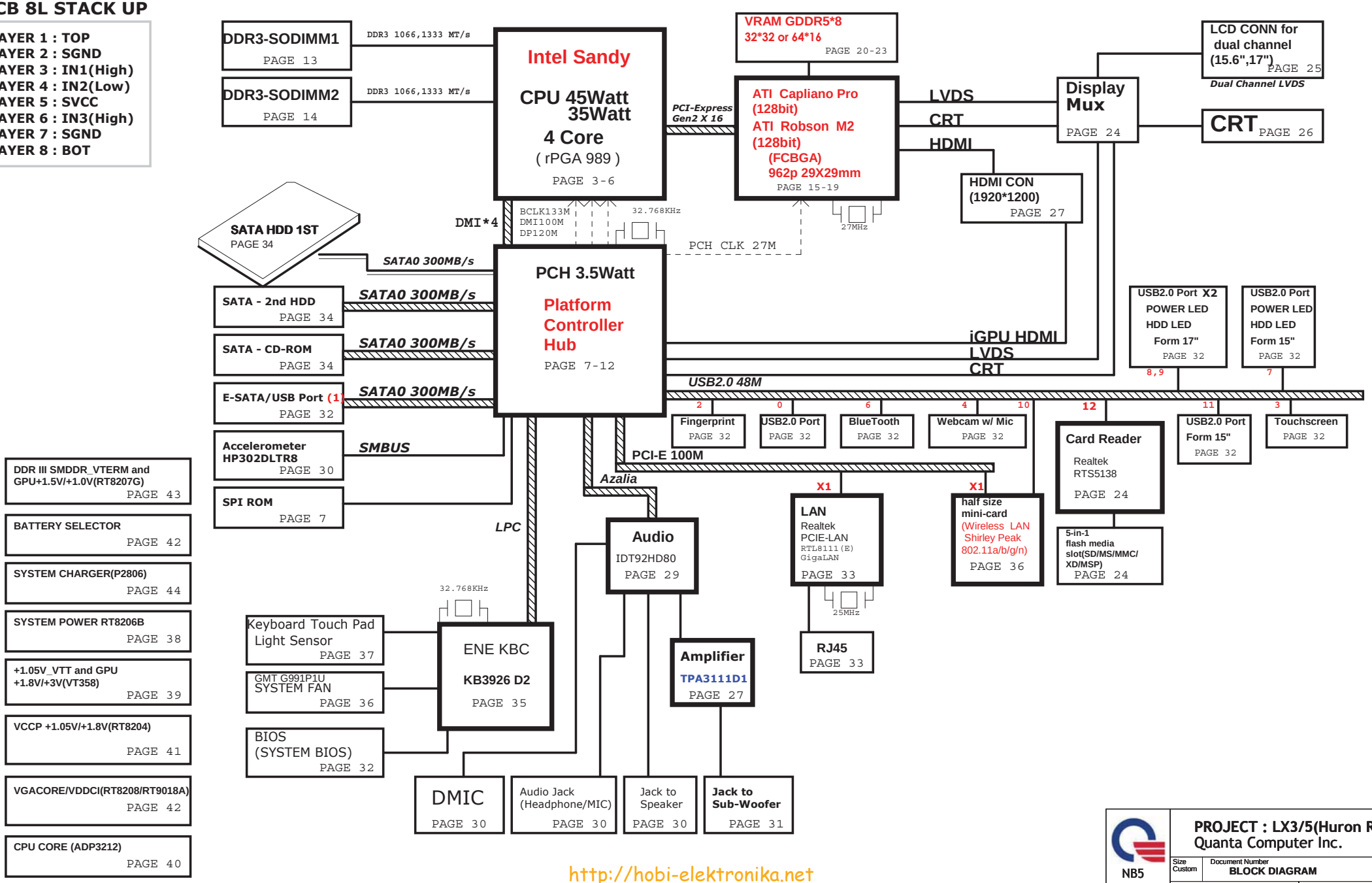
LX3/5 (Huron River) BLOCK DIAGRAM

Dis.
PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : IN3(High)
LAYER 7 : SGND
LAYER 8 : BOT



NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Friday, October 01, 2010 Sheet 1 of 47

4/7 DB del for PDC update.

NB5

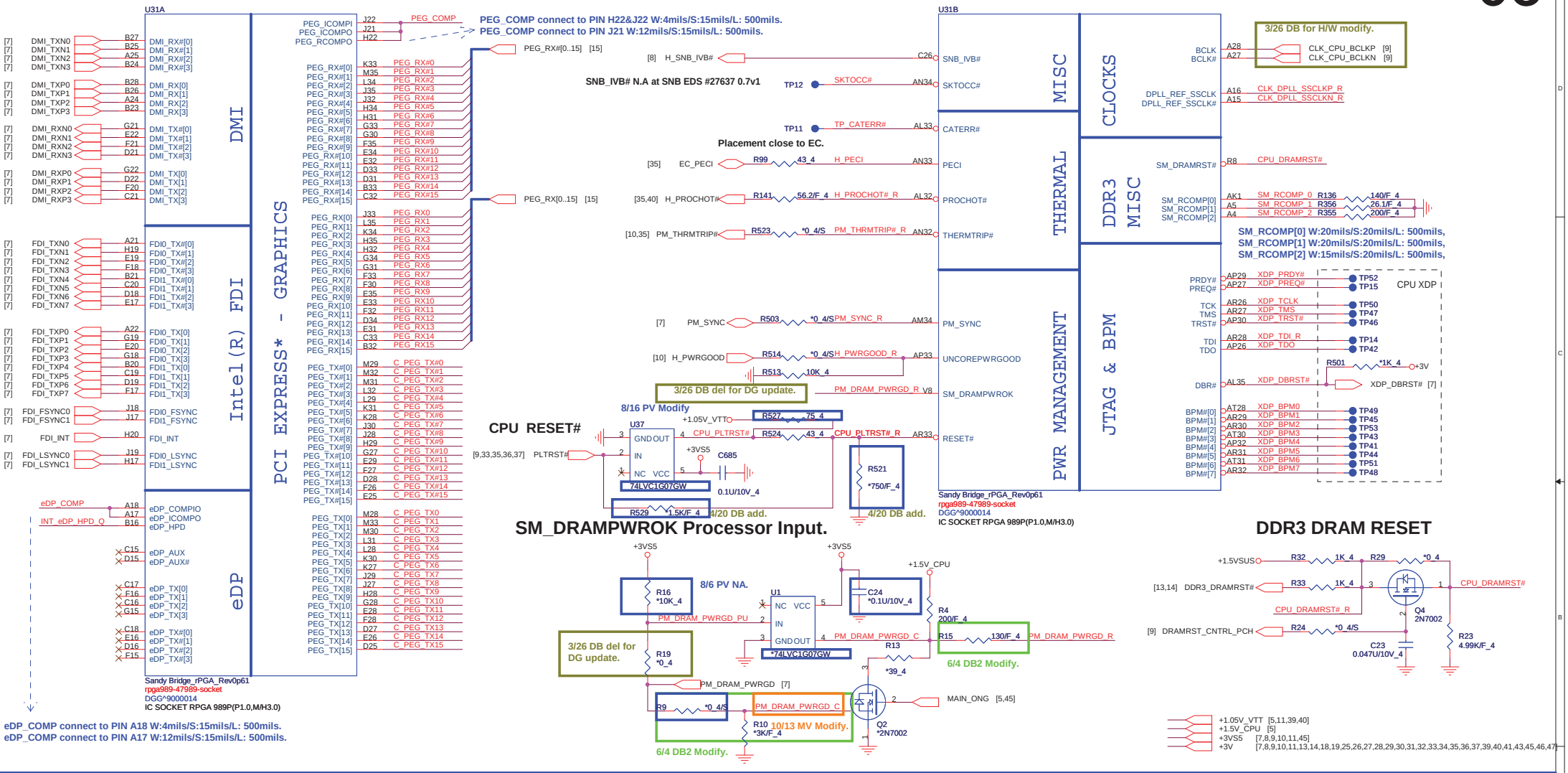
PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Gen(9LRS3197)/HOLES	1A

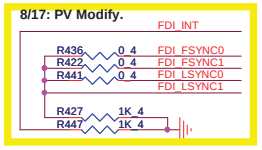
Date: Friday, October 01, 2010 | Sheet 2 of 47

Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)

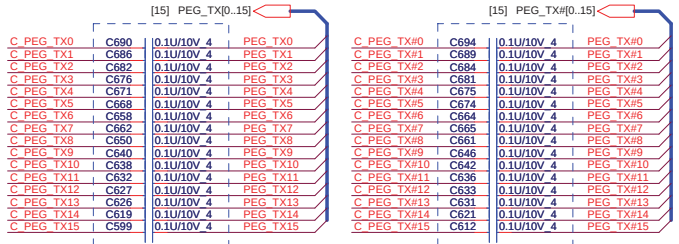


FDI disable (DIS only stuff)

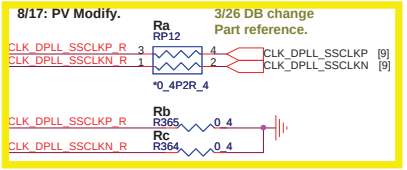


FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 disable (UMA only remove)

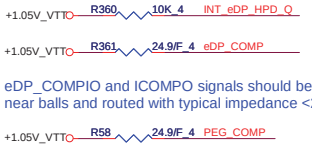


Embedded Display PLL Clock



	Ra	Rb	Rc
DIS	NC	Stuff	Stuff
SG/UMA	Stuff	NC	NC

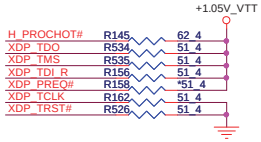
DP & PEG Compensation



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)



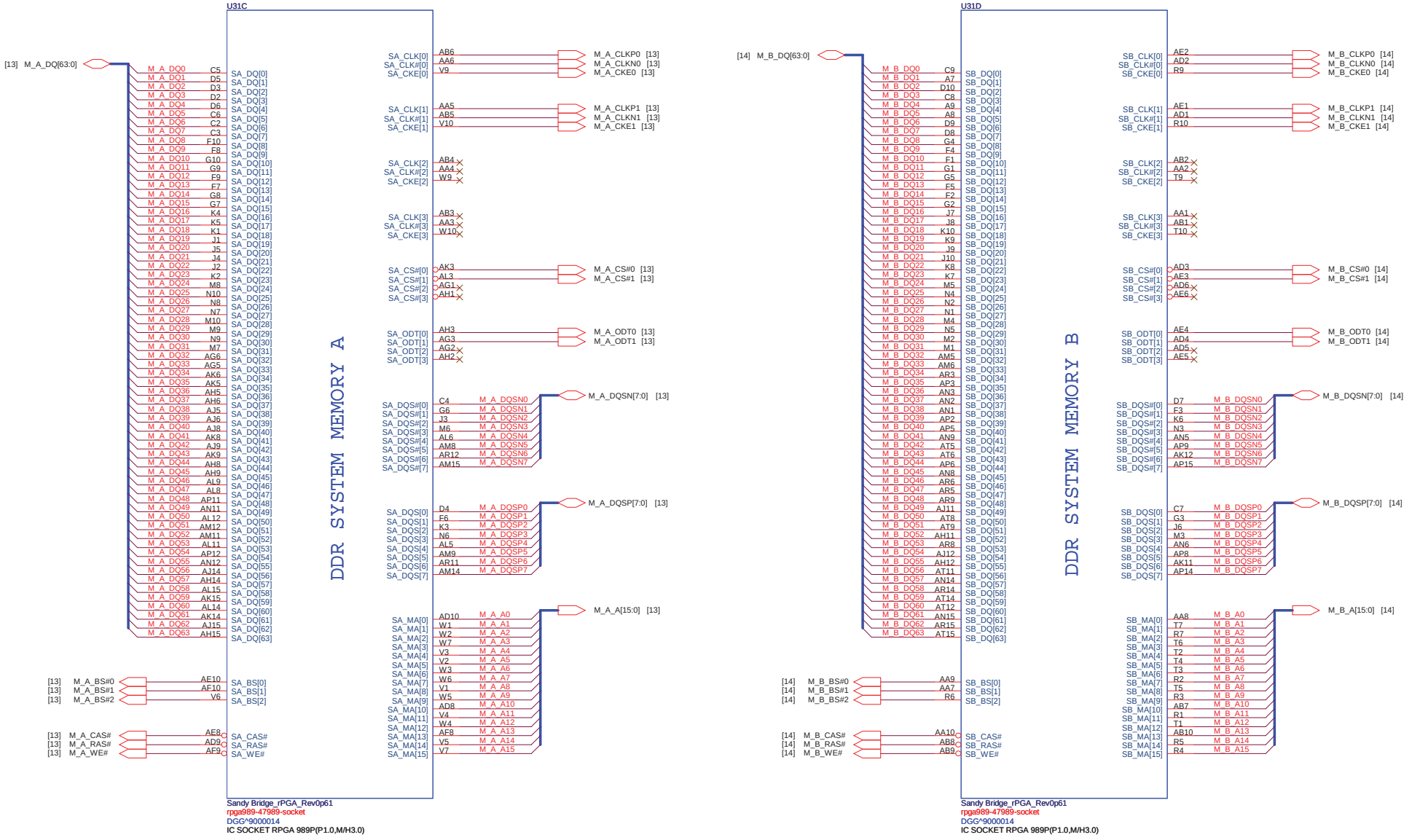
NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 1/4 (PCIE&DMI&FDI)	1A

Date: Wednesday, October 13, 2010 Sheet 3 of 47

Sandy Bridge Processor (DDR3)



NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 2/4 (DDR3 I/F)	1A

Date: Wednesday, October 13, 2010 Sheet 4 of 47

Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

9/29 MV for Power Modify.

05

U31F

SNB: 55A

+VCC_CORE

C596 22U/6.3V_8 C623 22U/6.3V_8 C586 22U/6.3V_8
C574 22U/6.3V_8 C564 22U/6.3V_8 C555 22U/6.3V_8
C577 22U/6.3V_8 C575 22U/6.3V_8 C132 22U/6.3V_8
C179 22U/6.3V_8 C95 22U/6.3V_8 C587 22U/6.3V_8
C67 22U/6.3V_8 C635 *22U/6.3VS_8 C85 22U/6.3V_8
C126 22U/6.3V_8 C106 22U/6.3V_8 C147 22U/6.3V_8
C122 22U/6.3V_8 C99 22U/6.3V_8 C76 22U/6.3V_8
C643 *22U/6.3VS_8 C672 *22U/6.3VS_8 C558 22U/6.3V_8
C576 22U/6.3V_8 C617 22U/6.3V_8 C110 22U/6.3V_8
C477 22U/6.3VS_8 C557 22U/6.3VS_8 C660 *22U/6.3VS_8

22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4

3/26 DB change 10U FP to 0805.

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

SNB: 8.5A

+1.05V_VTT

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

C71 22U/6.3VS_8 C69 22U/6.3VS_8 C541 22U/6.3VS_8
C131 22U/6.3VS_8 C86 22U/6.3VS_8 C176 22U/6.3VS_8
C70 *22U/6.3VS_8 C105 22U/6.3VS_8 C585 22U/6.3VS_8
C597 *22U/6.3VS_8 C94 *22U/6.3VS_8 C30 *22U/6.3VS_8
C547 22U/6.3VS_8 C31 *22U/6.3VS_8 C149 *22U/6.3VS_8
C68 *22U/6.3VS_8 C563 22U/6.3VS_8 C120 *22U/6.3VS_8
C573 *22U/6.3VS_8 C552 22U/6.3VS_8 C63 22U/6.3VS_8

5/14 modify

22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

+1.05V_VTT_40 R59 *0_4/S

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

3/26 DB Modify.

VCC_SENSE AJ35 R137 100_4 +VCC_CORE
VSS_SENSE AJ34 VCC_SENSE [40,46]
VSS_SENSE [40,46]
R135 100_4
VCCIO_SENSE B10 VCCP_SENSE [39]
VSSIO_SENSE A10 VSSP_SENSE TP37

Trace Route to Power IC area.

+VCC_CORE [40]
+VCC_GFX [40]
+VCCSA [41]
+1.05V_VTT [3,11,39,40]
+1.5V_CPU [3]
+1.5V_CPU [3]
+1.5VSUS [3,11,13,14,43,45]

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGQ^9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

9/26: MV Modify

SNB: 21.5A

+VCC_GFX

C591 *22U/6.3V_8 C130 *22U/6.3V_8
C145 *22U/6.3V_8 C177 *22U/6.3V_8
C143 *22U/6.3V_8 C590 *22U/6.3V_8
C178 *22U/6.3V_8 C123 *22U/6.3V_8
C589 *22U/6.3V_8 C121 *22U/6.3V_8
C133 *22U/6.3V_8 C598 *22U/6.3V_8

5/4: add C8260/ C8322

8/17: PV Modify

Ra R522 0_4

	DIS	SG/UMA
Ra	Stuff	NC

SNB: 1.5A

+1.8V

C492 10U/6.3V_6 C495 1U/6.3V_4 C494 1U/6.3V_4 C486 330U/2V_7343

330uF x1, 10uF_8 x1, 1uF_4 x2 Socket BOT edge.

3/26 DB change 10U FP to 0805.

6/7 DB2 Modify

U31G

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

GRAPHICS

VCCPLL1 VCCPLL2 VCCPLL3

1.8V RAIL

SENSE LINES

VAXG_SENSE
VSSAXG_SENSE

3/26 DB Modify.

R130 *100_4 +VCC_GFX

	DIS	SG/UMA
R130	NC	Stuff

VCC_AXG_SENSE [40,46]
VSS_AXG_SENSE [40,46]
R124 100_4

VREF

SM_VREF AL1

+VDDR_REF_CPU

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

R175 *0_8 DDR_VTTREF [13,14,43]
R170 100K_4
Q13 2N7002
MAIND MAIND [45]

DDR3 -1.5V RAILS

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15

5/14 modify

SNB: 5A

+1.5V_CPU

C89 10U/6.3V_6 C109 10U/6.3V_8 C155 10U/6.3V_6 C112 10U/6.3V_6

4/27: layout modify

5/23: na

C127 10U/6.3V_6 C174 10U/6.3V_6 C714 *330U_2.5V_5.0x5.9_ESR10m

330uF x1, 10uF_8 x6 Socket BOT edge.

3/26 DB change 10U FP to 0805.

SA RAIL

VCCSA1 VCCSA2 VCCSA3 VCCSA4 VCCSA5 VCCSA6 VCCSA7 VCCSA8

SNB: 6A

+VCCSA

C549 10U/6.3V_8 C482 10U/6.3V_8 C545 10U/6.3V_8 C485 *10U/6.3V_8

330uF x1, 10uF_8 x1 Socket BOT edge, 10uF_8 x2 Socket BOT cavity.

3/26 DB change 10U FP to 0805.

MISC

VCCSA_SENSE H23 VCCUSA_SENSE_R R358 *0_4/S VCCUSA_SENSE [41]

FC_C22 C22 H_FC_C22 R363 10K_4
VCCSA_VID1 C24 VCCSA_SEL [41]
R357 10K_4

5/11: Add for intel CRB

+1.5V_CPU R747 0_8 +1.5V

5/13: modify 40mile routing

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGQ^9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

Layout note: need routing together and ALERT need between CLK and DATA.

SVID CLK

Place PU resistor close to VR

R120 *54.9/F_4 +1.05V_VTT

H_CPU_SVIDCLK VR_SVID_CLK [40]

3/26 DB Modify.

SVID DATA

+1.05V_VTT +1.05V_VTT

Place PU resistor close to CPU

R108 130/F_4

R100 *130/F_4

Place PU resistor close to VR

H_CPU_SVIDDAT VR_SVID_DATA [40]

3/26 DB Modify. 5/12: modify

Place PU resistor close to CPU

C921 *0.1U/10V_4 10/01: modify

SVID ALERT

+1.05V_VTT R96 75_4

3/26 DB Modify.

H_CPU_SVIDALRT# R89 43_4 VR_SVID_ALERT# [40]

+1.5VSUS JP1 *SOLDERJUMPER-2 +1.5V_CPU

Q39 AON7410

R2 220_8

MAIND

4/27: layout modify

C18 *470P/50V_4

Q1 2N7002

MAIN_ONG [3,45]

5/6: modify

C710 0.1U/10V_4
C712 0.1U/10V_4
C715 0.1U/10V_4
C699 0.1U/10V_4

3/26 DB add for Intel. Placement close to CPU.

+1.5VSUS

CPU VDDQ

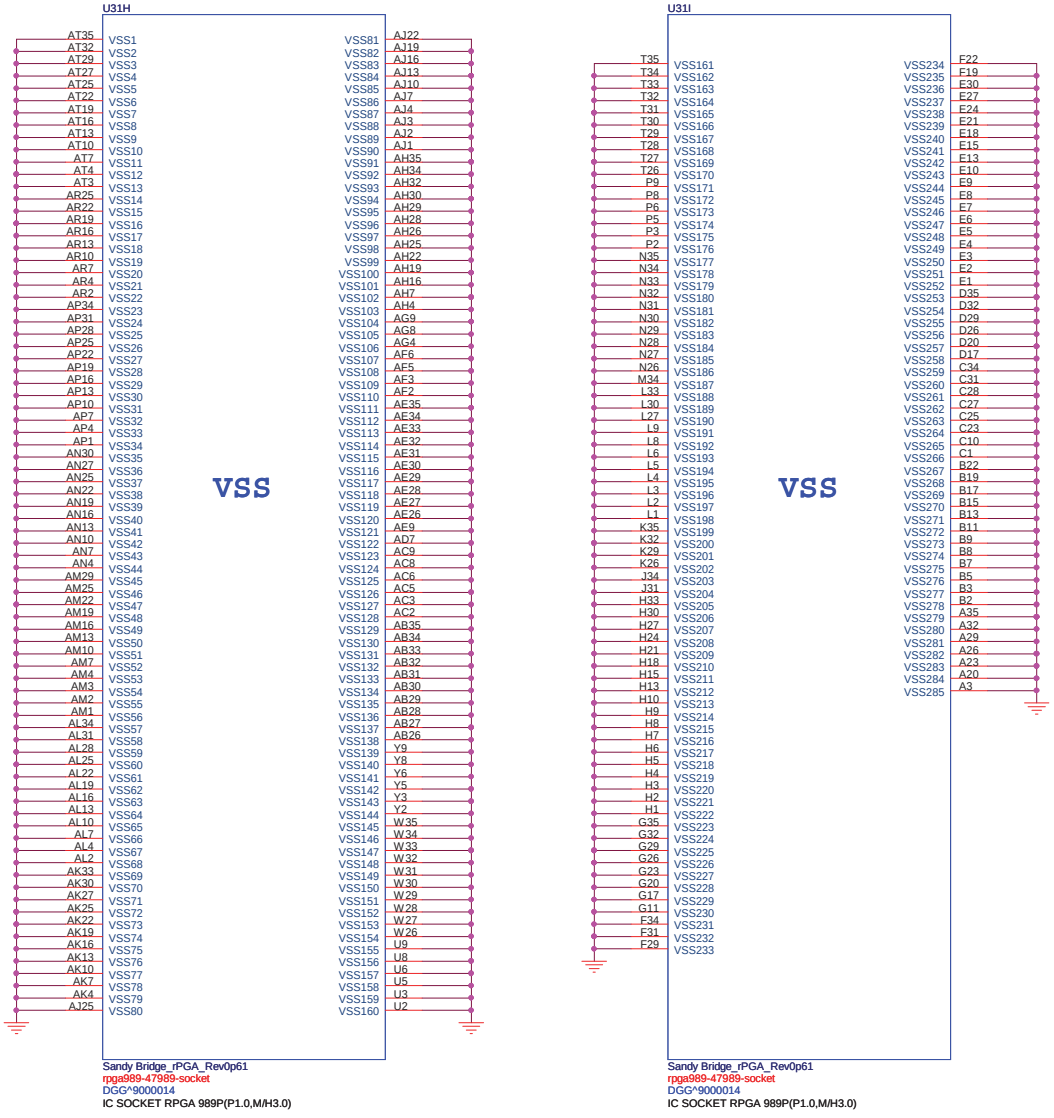
NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

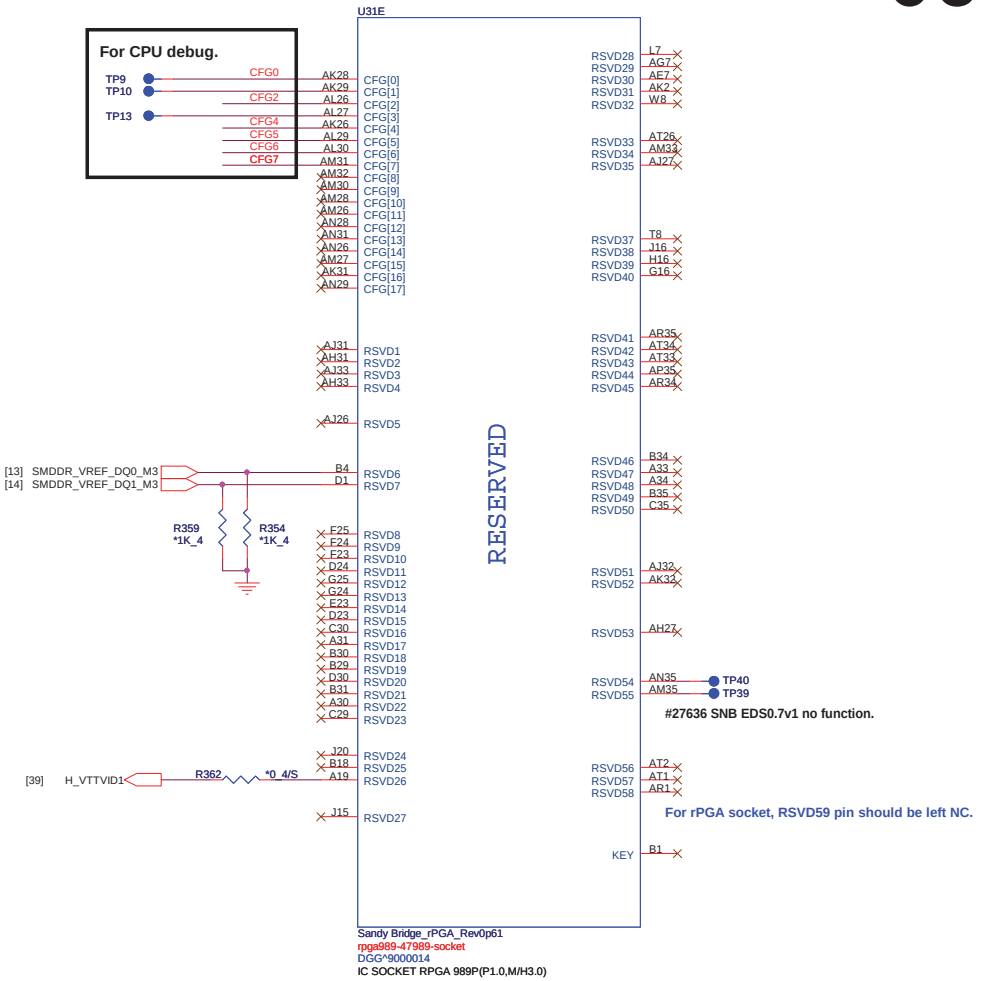
Size	Document Number	Rev
Custom	SNB 3/4 (POWER)	1A

Date: Wednesday, October 13, 2010 Sheet 5 of 47

Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)



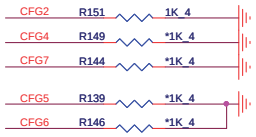
Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

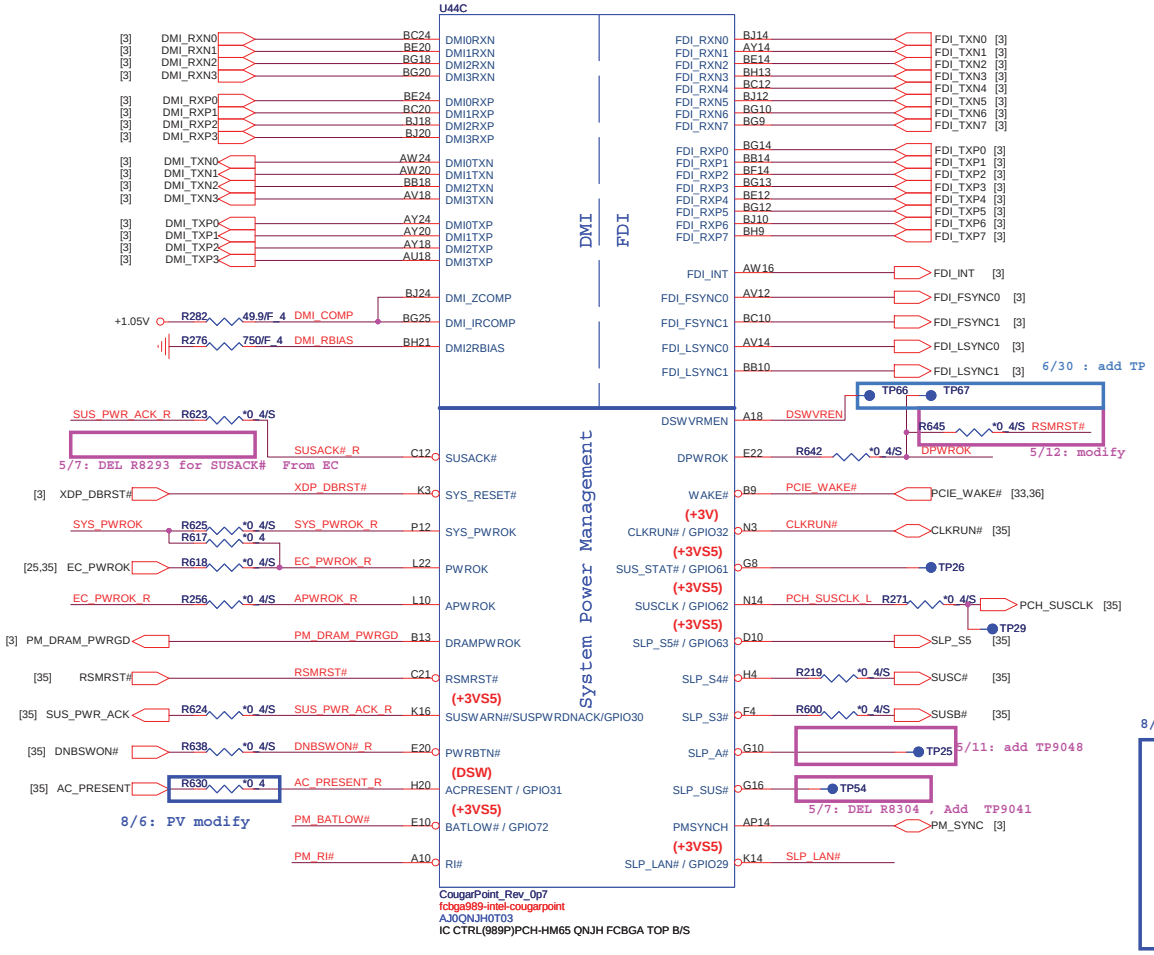
Size	Document Number	Rev
Custom	SNB 4/4 (GND)	1A

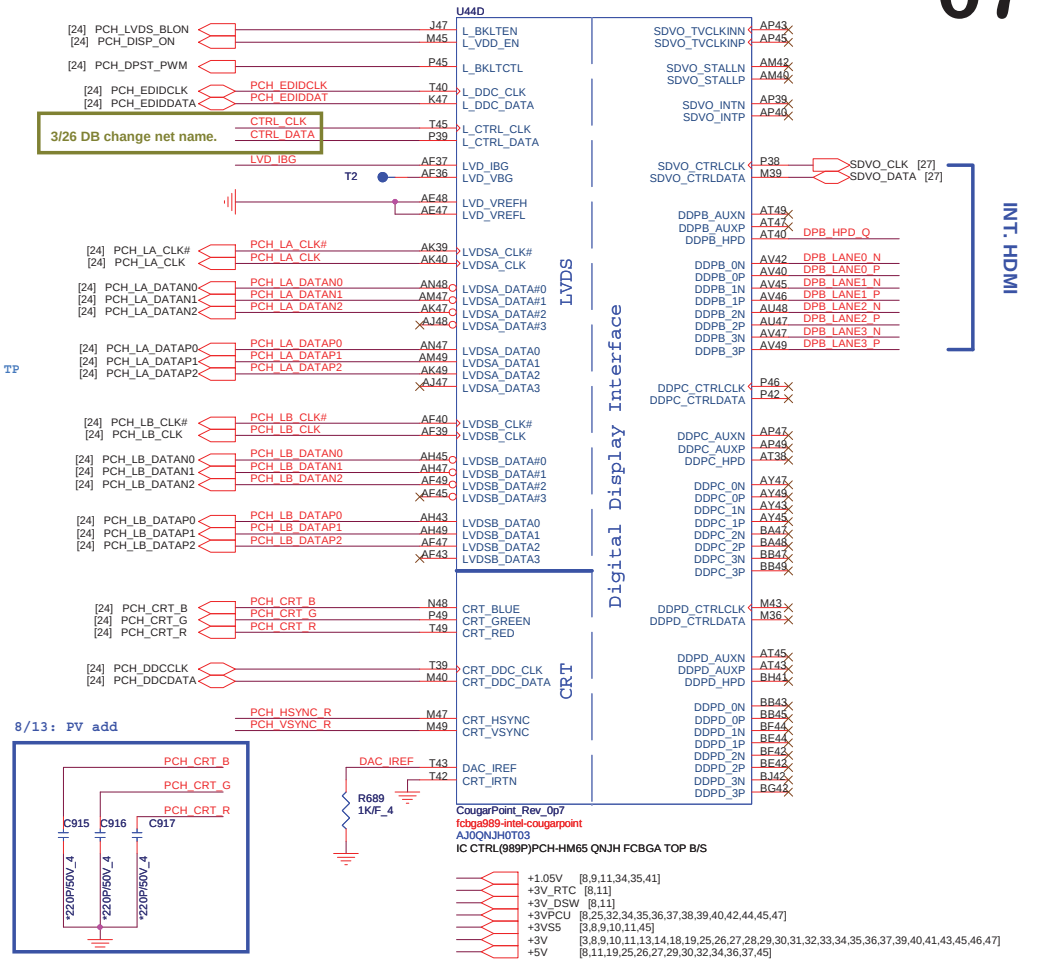
Date: Wednesday, October 13, 2010 | Sheet 6 of 47

Cougar Point (DMI,FDI,PM)

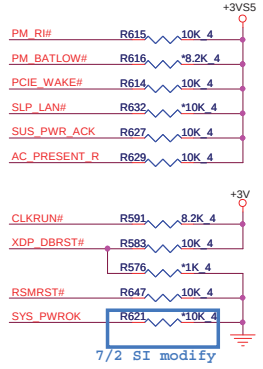
Cougar Point (LVDS,DDI)

07

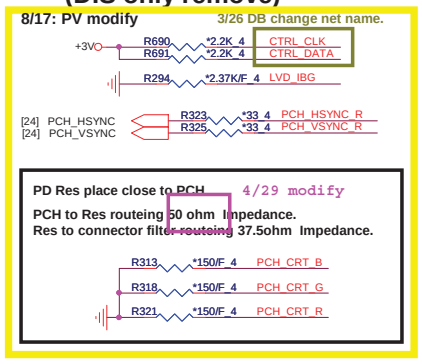




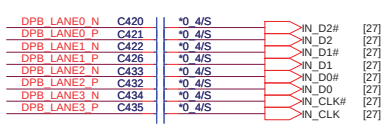
PCH Pull-high/low(CLG)



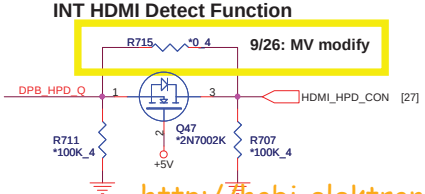
INT LVDS & CRT disable (DIS only remove)



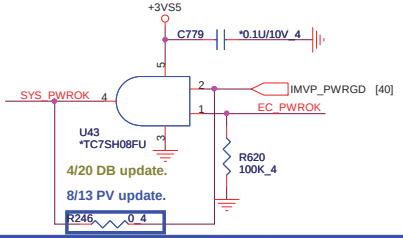
INT HDMI disable (DIS only remove)



INT HDMI Detect Function

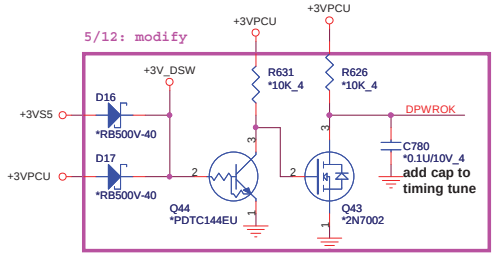


System PWR_OK(CLG)



On Die DSW VR Enable
High = Enable (Default)
Low = Disable

DPWROK FOR DSW

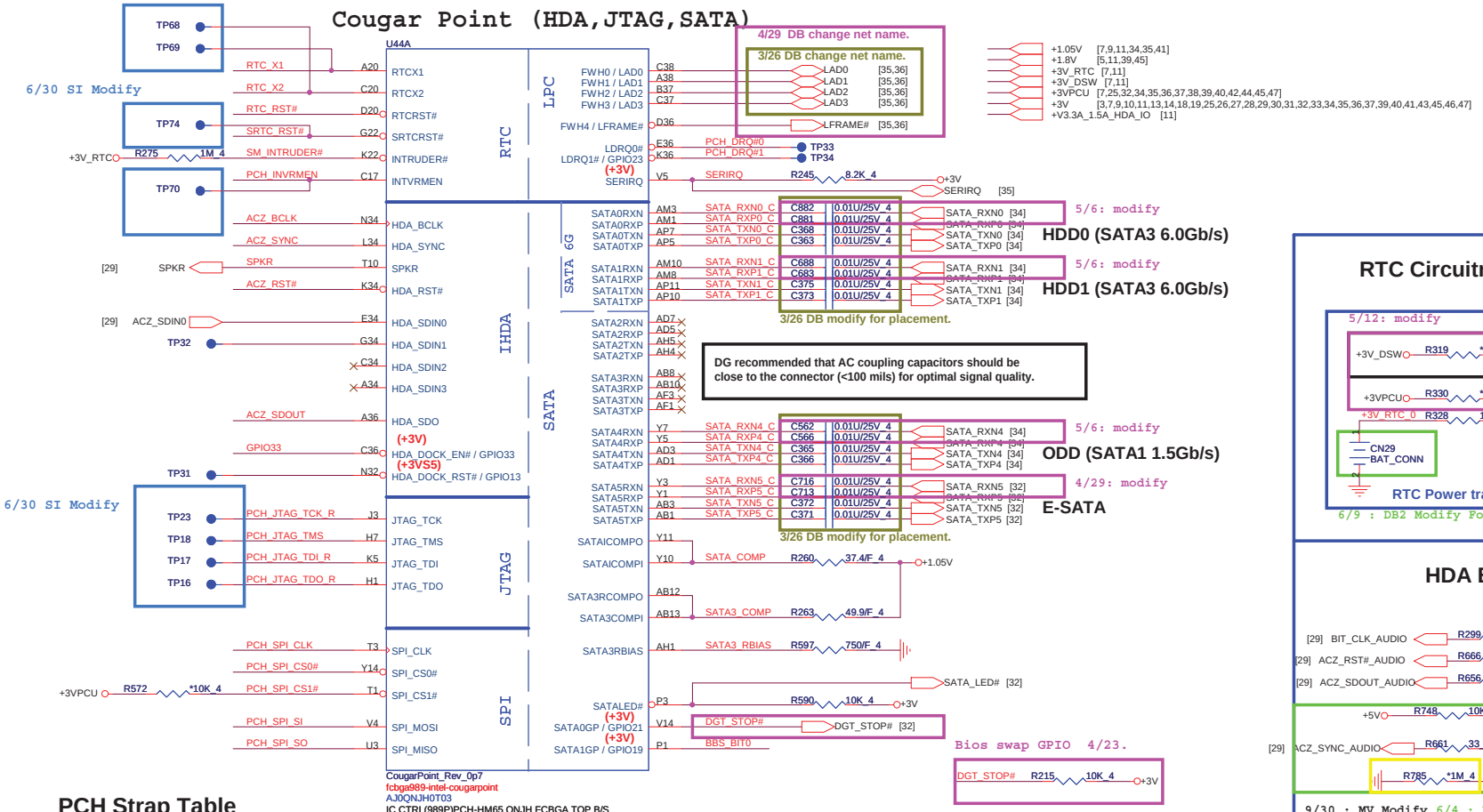


NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A
Date: Wednesday, October 13, 2010	Sheet 7 of 47	

Cougar Point (HDA,JTAG,SATA)



6/30 SI Modify

6/30 SI Modify

4/29 DB change net name.

3/26 DB change net name.

5/6: modify

HDD0 (SATA3 6.0Gb/s)

5/6: modify

HDD1 (SATA3 6.0Gb/s)

3/26 DB modify for placement.

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

5/6: modify

ODD (SATA1 1.5Gb/s)

4/29: modify

E-SATA

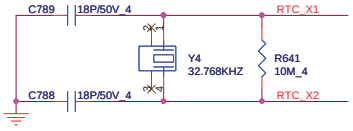
3/26 DB modify for placement.

Bios swap GPIO 4/23.

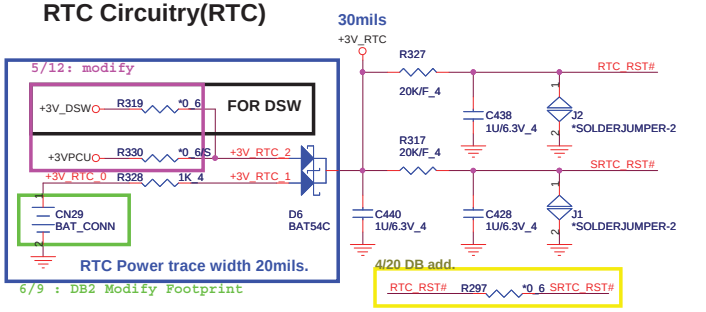
CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QNJH0T03
IC CTRL(989P)PCH-HM65 QNJH FCBGA TOP B/S

RTC Clock 32.768KHz

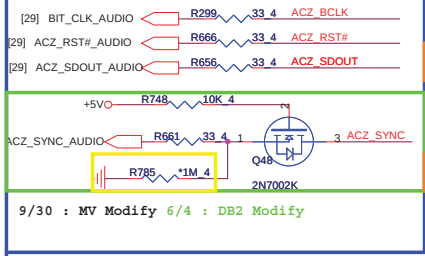
08



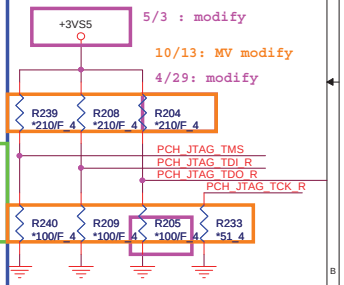
RTC Circuitry(RTC)



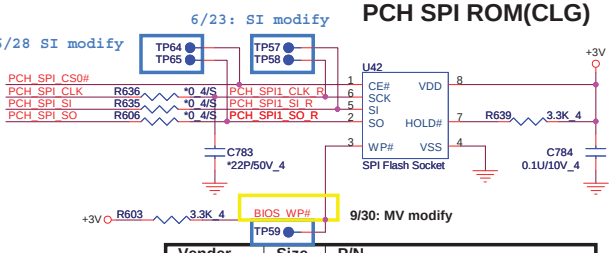
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

PCH Strap Table

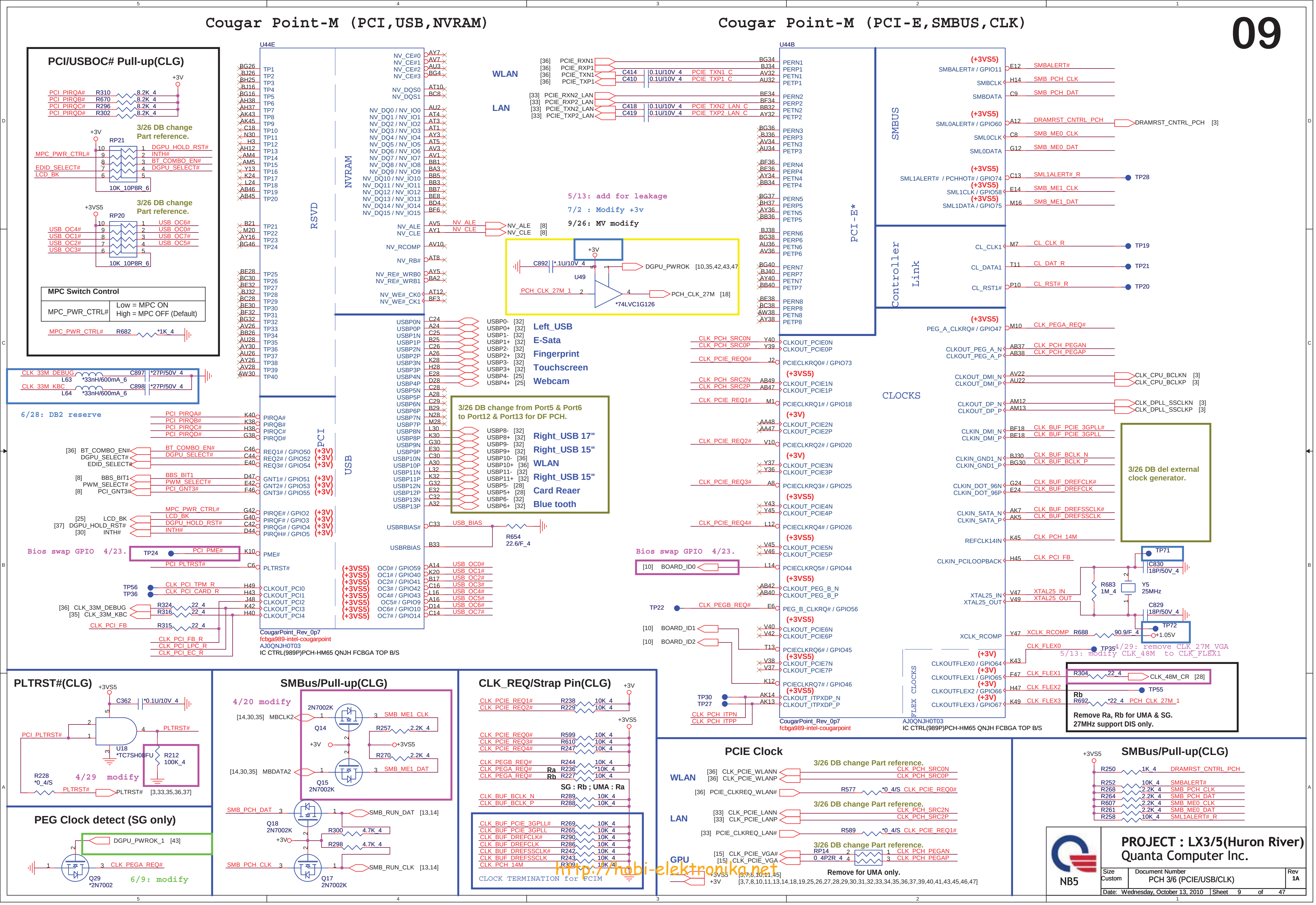
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR Different from Calpella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R568 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R687 *1K_4, R700 10K_4, PCI_GNT3# [9], Bios request, for can't boot Capella 4/28.
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R640 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R659 0_4 BIOS_WP# 9/30: MV modify
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1, GNT0# 1 → Boot Location SPI	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK	GNT1# 0, GNT0# 0 → Boot Location LPC	R573 *1K_4, R686 *1K_4, BBS_BIT0, BBS_BIT1 [9]
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R596 *1K_4 NV_ALE [9]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm 4/29 modify	+1.8V R595 2.2K_4, R609 4.7K_4, NV_CLE [9], H_SNB_IVB# [3] N.A at CPT EDS 0.7
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VS5 R307 1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	[35] GPIO33_E ACZ_SDOUT R662 *1K_4 +V3.3A_1.5A_HDA_IO 8/12 PV Modify.
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R619 *1K_4 ICC_EN# [10] 4/29 reserve.
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R608 *1K_4 PLL_ODVR_EN [10]
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R634 1K_4 +3V

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A

Date: Wednesday, October 13, 2010 Sheet 8 of 47

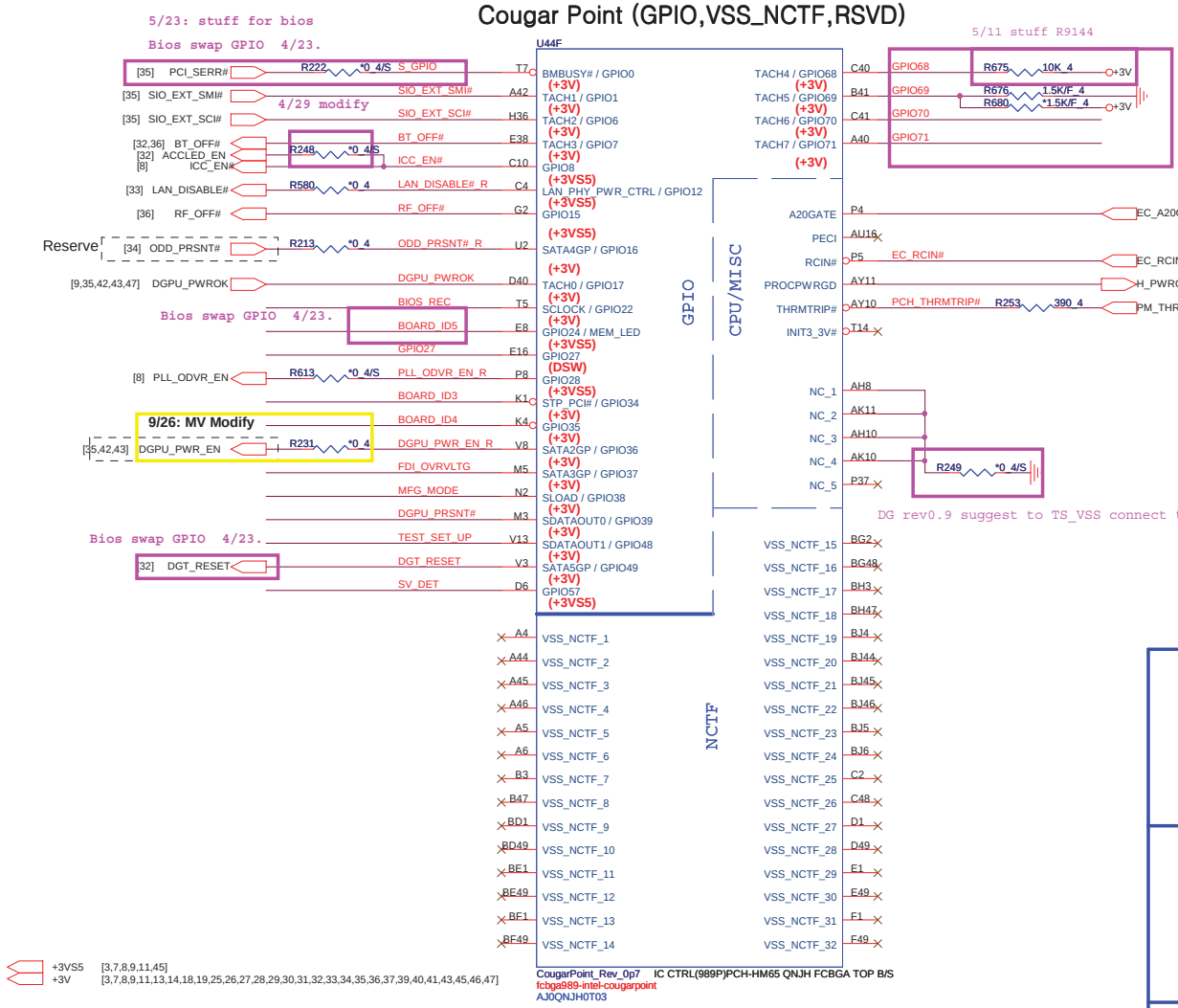


Cougar Point-M (PCI,USB,NVRAM)
Cougar Point-M (PCI-E,SMBUS,CLK)
09
PCI/USBOC# Pull-up(CLG)
3/26 DB change Part reference.
3/26 DB change Part reference.
MPC Switch Control
MPC_PWR_CTRL#
Low = MPC ON
High = MPC OFF (Default)
6/28: DB2 reserve
Bios swap GPIO 4/23.
U44E
RSVD
NVRAM
PCI
USB
5/13: add for leakage
7/2 : Modify +3v
9/26: MV modify
3/26 DB change from Port5 & Port6 to Port12 & Port13 for DF PCH.
Left_USB
E-Sata
Fingerprint
Touchscreen
Webcam
Right_USB 17"
Right_USB 15"
WLAN
Right_USB 15"
Card Reaer
Blue tooth
CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QNJH0T03
IC CTRL(989P)PCH-HM65 QNJH FCBGA TOP B/S
U44B
WLAN
LAN
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
3/26 DB del external clock generator.
Bios swap GPIO 4/23.
4/29: remove CLK_27M_VGA
5/13: modify CLK_48M to CLK_FLEX1
Remove Ra, Rb for UMA & SG.
27MHz support DIS only.
PLTRST#(CLG)
4/29 modify
PEG Clock detect (SG only)
6/9: modify
SMBus/Pull-up(CLG)
4/20 modify
CLK_REQ/Strap Pin(CLG)
SG : Rb ; UMA : Ra
CLOCK TERMINATION for FCIM
PCIE Clock
WLAN
LAN
GPU
3/26 DB change Part reference.
3/26 DB change Part reference.
3/26 DB change Part reference.
Remove for UMA only.
SMBus/Pull-up(CLG)
http://hobi-elektronika.net
PROJECT : LX3/5(Huron River)
Quanta Computer Inc.
NB5
Size Custom
Document Number PCH 3/6 (PCI/USB/CLK)
Rev 1A
Date: Wednesday, October 13, 2010
Sheet 9 of 47

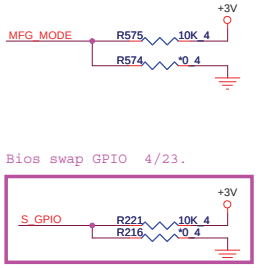
Cougar Point (GPIO,VSS_NCTF,RSVD)

Clock Gen Power OK (CLG)

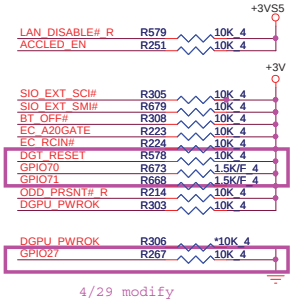
3/26 DB del external clock generator.

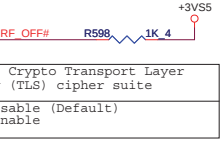


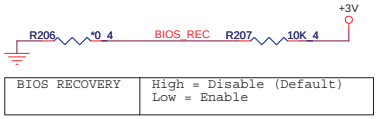
MFG-TEST

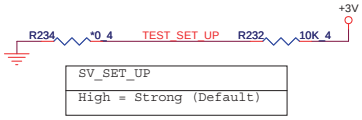


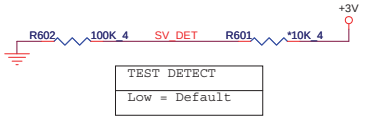
GPIO Pull-up/Pull-down(CLG)

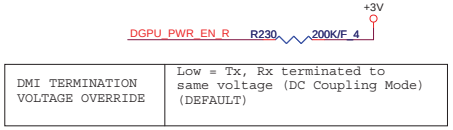


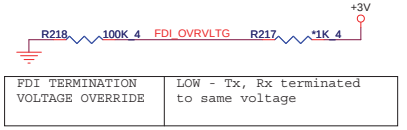




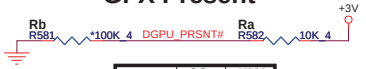








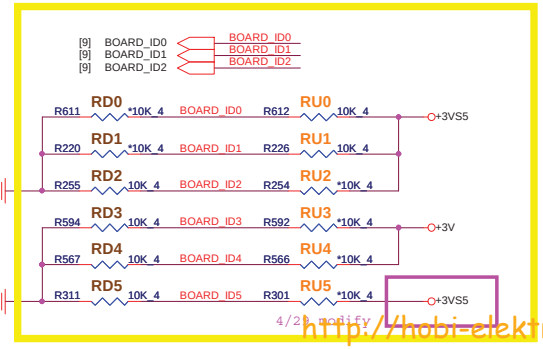
GFX Present



	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
LX3 UMA	0	0	0	0	0	0
LX5 UMA	0	0	0	0	0	1
LX3 Capilano XT	0	0	0	0	1	0
LX3 Capilano XT - SG	0	0	0	0	1	1
LX5 Capilano XT	0	0	0	1	0	0
LX5 Capilano XT - SG	0	0	0	1	0	1
LX5 DISCRETE SG/Subwoofer	0	0	0	1	1	0
LX5 DISCRETE Subwoofer	0	0	0	1	1	1



NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A

Date: Wednesday, October 13, 2010 Sheet 10 of 47

Cougar Point-M (POWER)

COUGAR POINT (POWER)

U44J

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | MISC | CPU | RTC | HDA

U44G

VCC CORE | CRT | LVDS | HVCMOS | DMI | VCCIO | SPI | NAND / FDI

5/12: modify

8/6: PV modify 4/29: modify

6/9: DB2 modify

7/1: SI DEL

1.01A (60mils)

1.3 A (60mils)

2.925 A (140mils)

119mA (20mils)

119mA (15mils)

266mA (20mils)

3mA (10mils)

1mA (10mils)

8/17: PV modify

60mA (10mils)

42mA (10mils)

190 mA (15mils)

20mA (10mils)

160mA (20mils)

65mA (10mils)

8mA (10mils)

55mA (10mils)

95mA (10mils)

1.01A (60mils)

10mA (10mils)

160mA (15mils)

(Mobile 1.5V)

5/14 modify

V_PROC_IO=1mA (10mils)

VCCRTC<1mA (10mils)

V5REF= 1mA

VCC5REFSUS=1mA

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QNJH0T03
IC CTRL(989P)PCH-HM65 QNJH FCBGA TOP B/S

+1.05V [7,8,9,34,35,41]
+1.05V_VTT [3,5,39,40]
+1.5VSUS [3,5,13,14,43,45]
+1.8V [5,8,39,45]

+3V_RTC [7,8]
+3V_DSW [7,8]
+3VS5 [3,7,8,9,10,45]
+3V [3,7,8,9,10,13,14,18,19,25,26,27,28,29,30,31,32,33,34,35,36,37,39,40,41,43,45,46,47]
+5VS5 [45]
+5V [7,8,19,25,26,27,29,30,32,34,36,37,45]

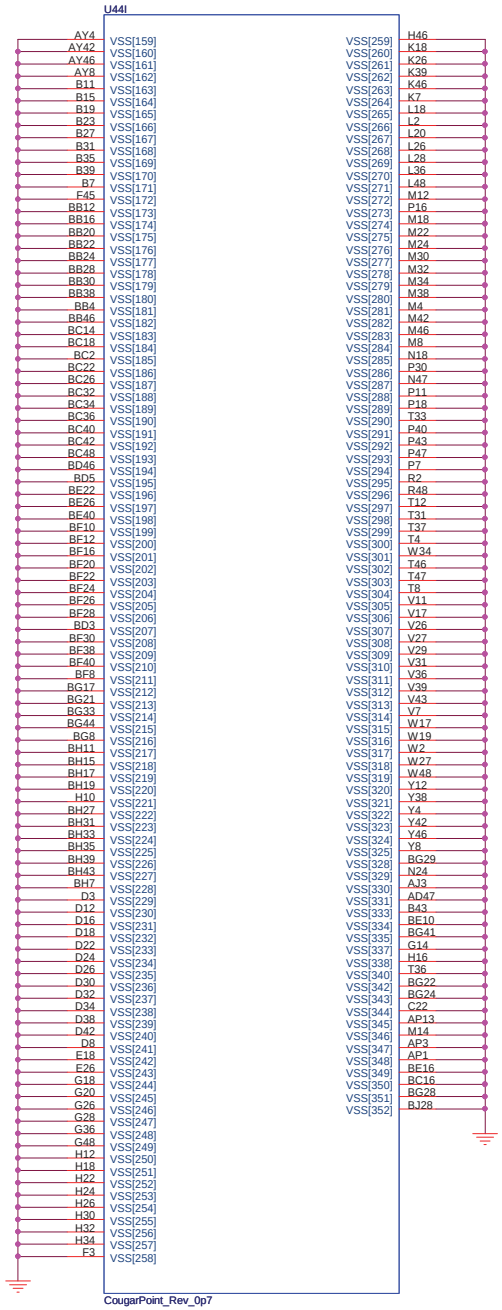
NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

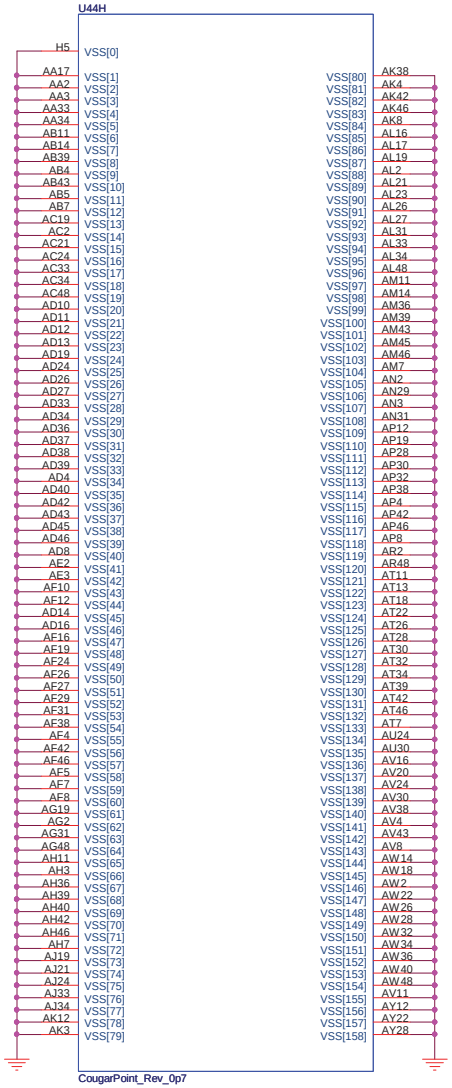
Size	Document Number	Rev
Custom	PCH 5/6 (POWER)	1A

Date: Wednesday, October 13, 2010 Sheet 11 of 47

IBEX PEAK-M (GND)



IBEX PEAK-M (GND)

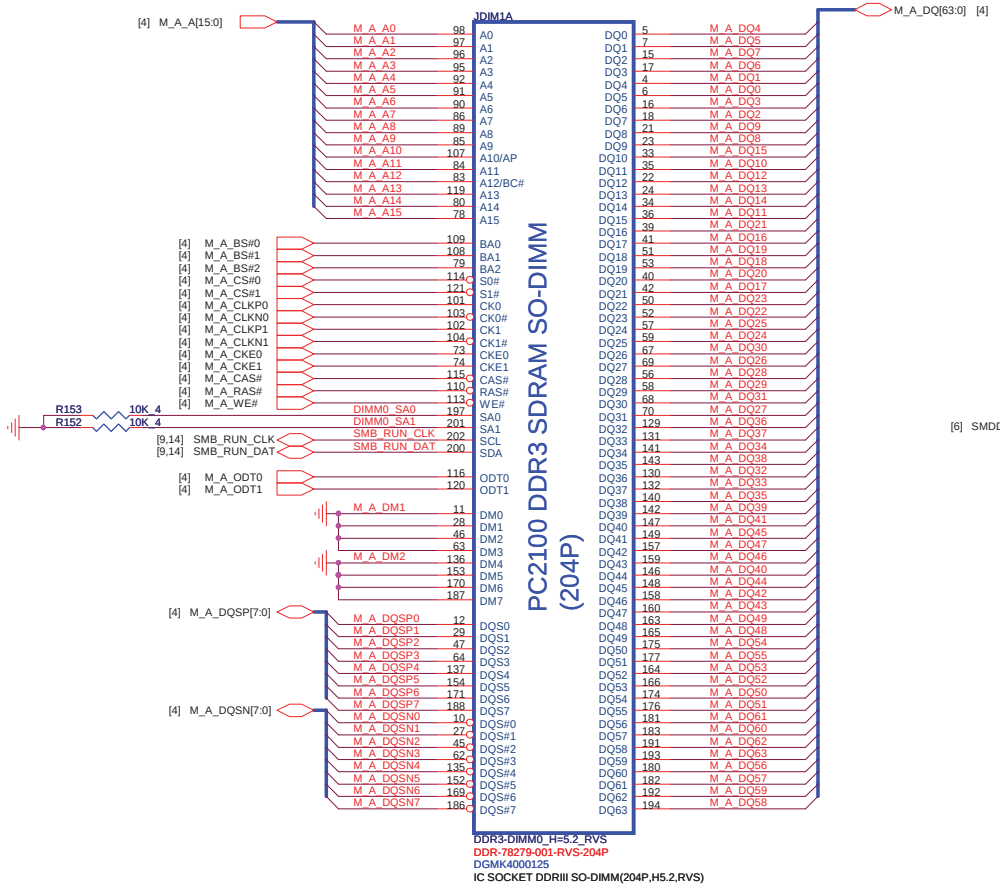


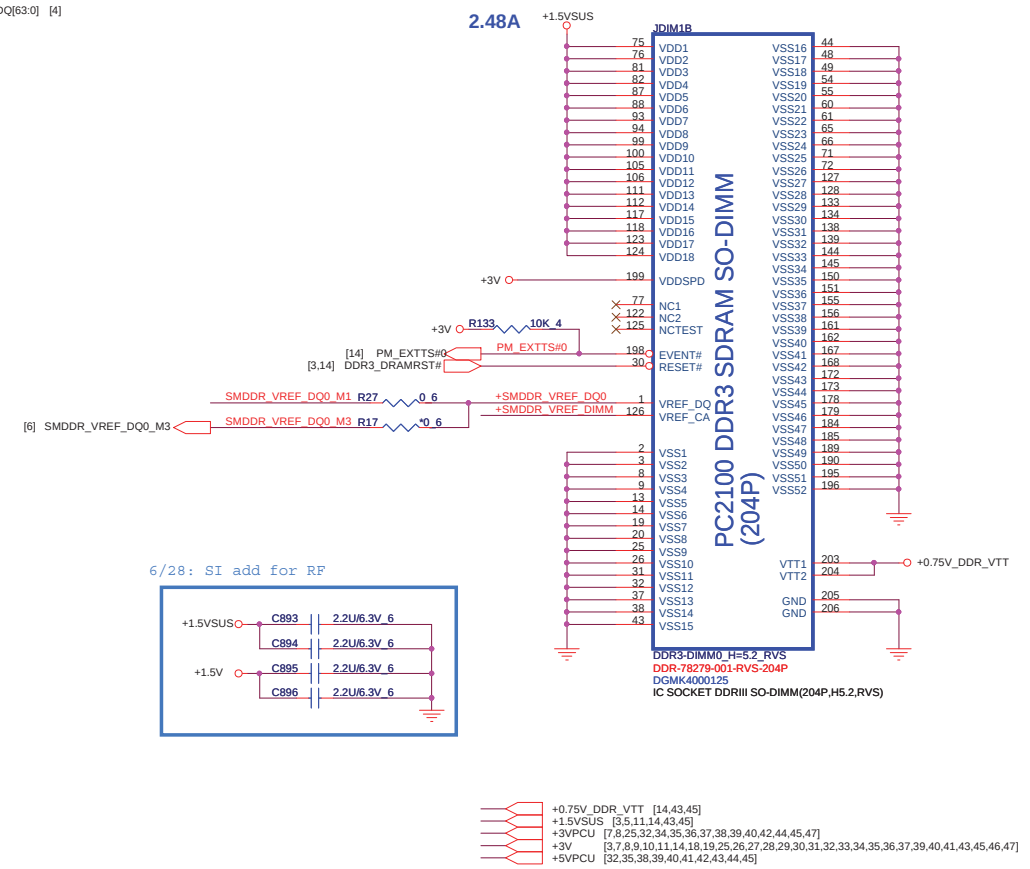
NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	1A

Date: Wednesday, October 13, 2010 Sheet 12 of 47



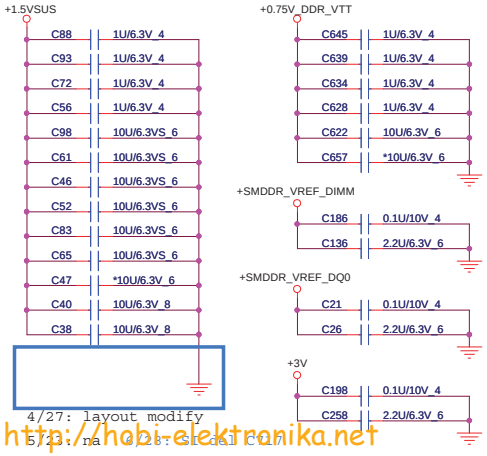


VREF DQ0 M2 Solution

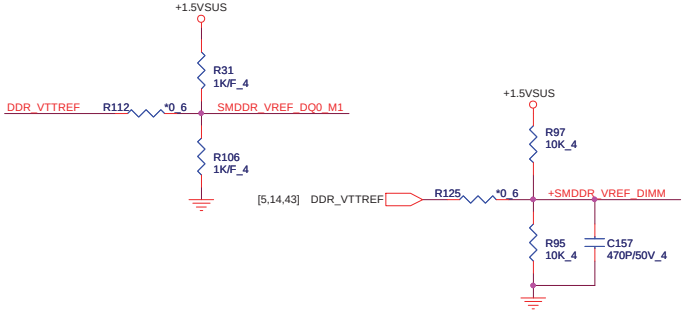
6/23 : Del M2 solution

4/29: reserve M2 solution

Place these Caps near So-Dimm0.



VREF DQ0 M1 Solution



NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (5.2H)	1A

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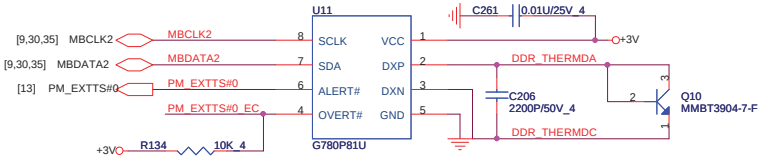
DDR3 Thermal Sensor

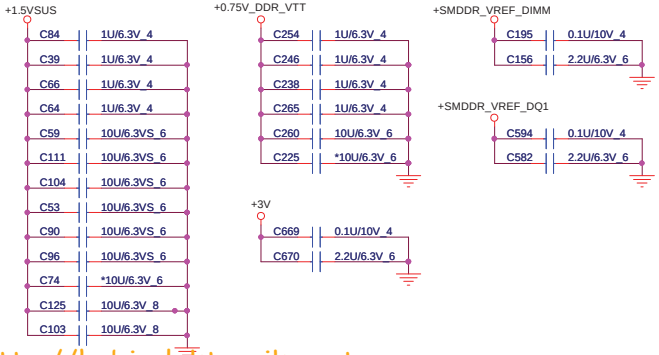


VREF DQ1 M2 Solution

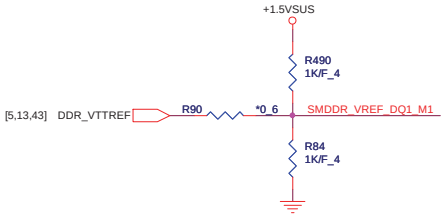
6/23 : Del M2 solution

4/29 reserve M2 solution

Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS (9.2H)	1A

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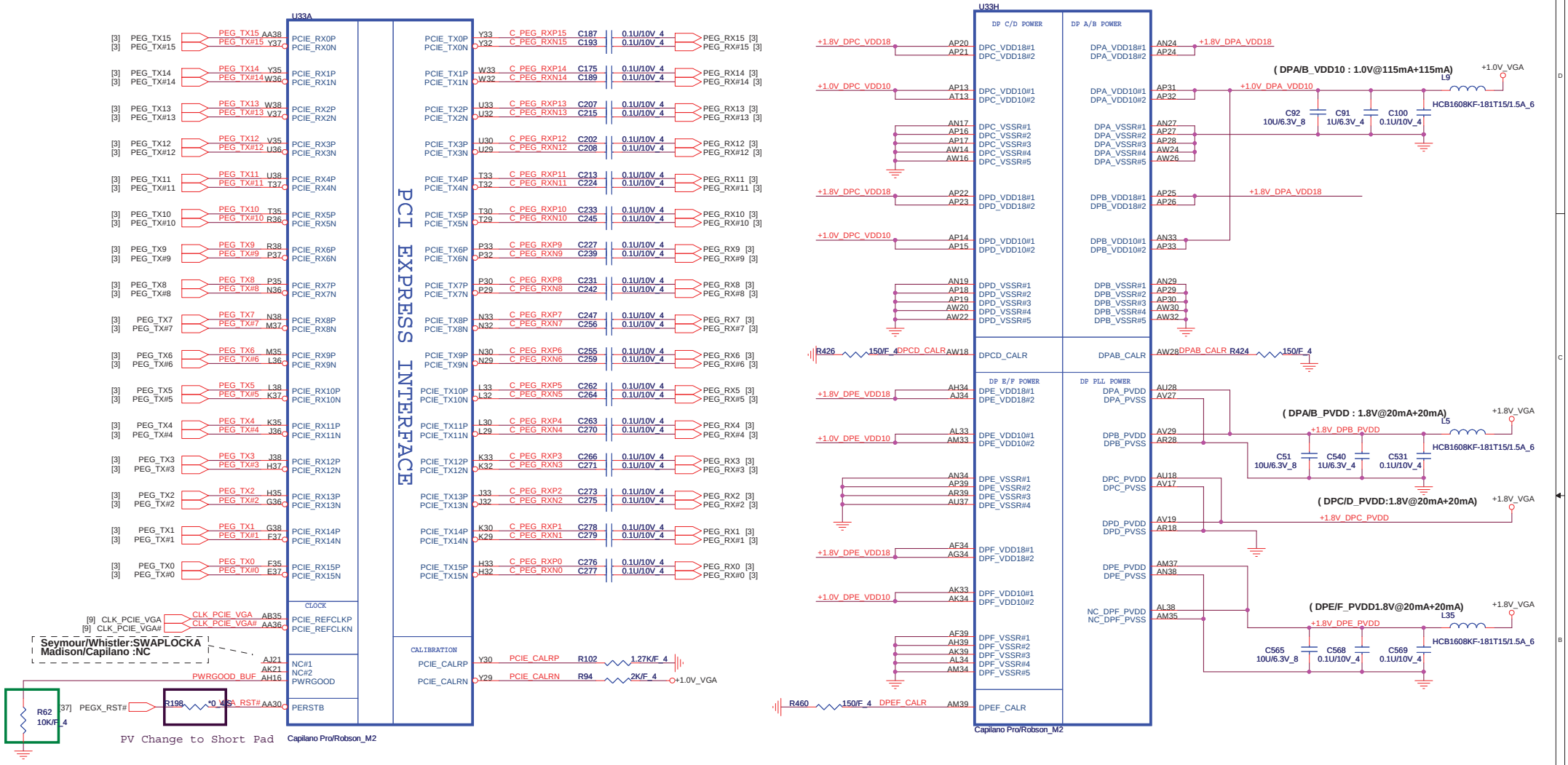
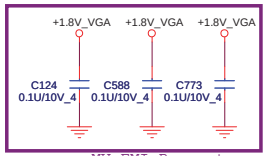
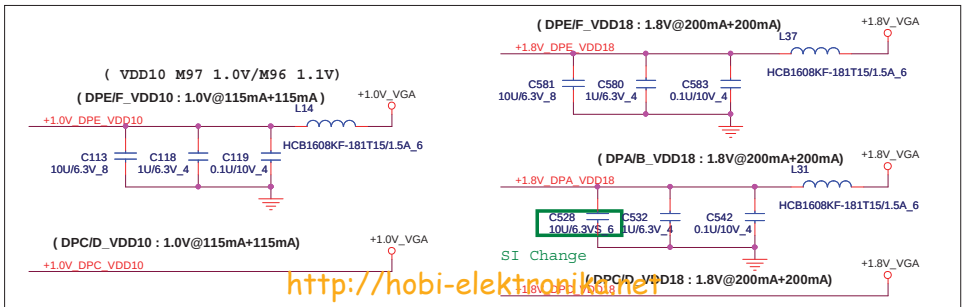




SI Del R43,R38,C57



+1.0V_VGA [17,19,43]
+1.8V_VGA [17,19,42]

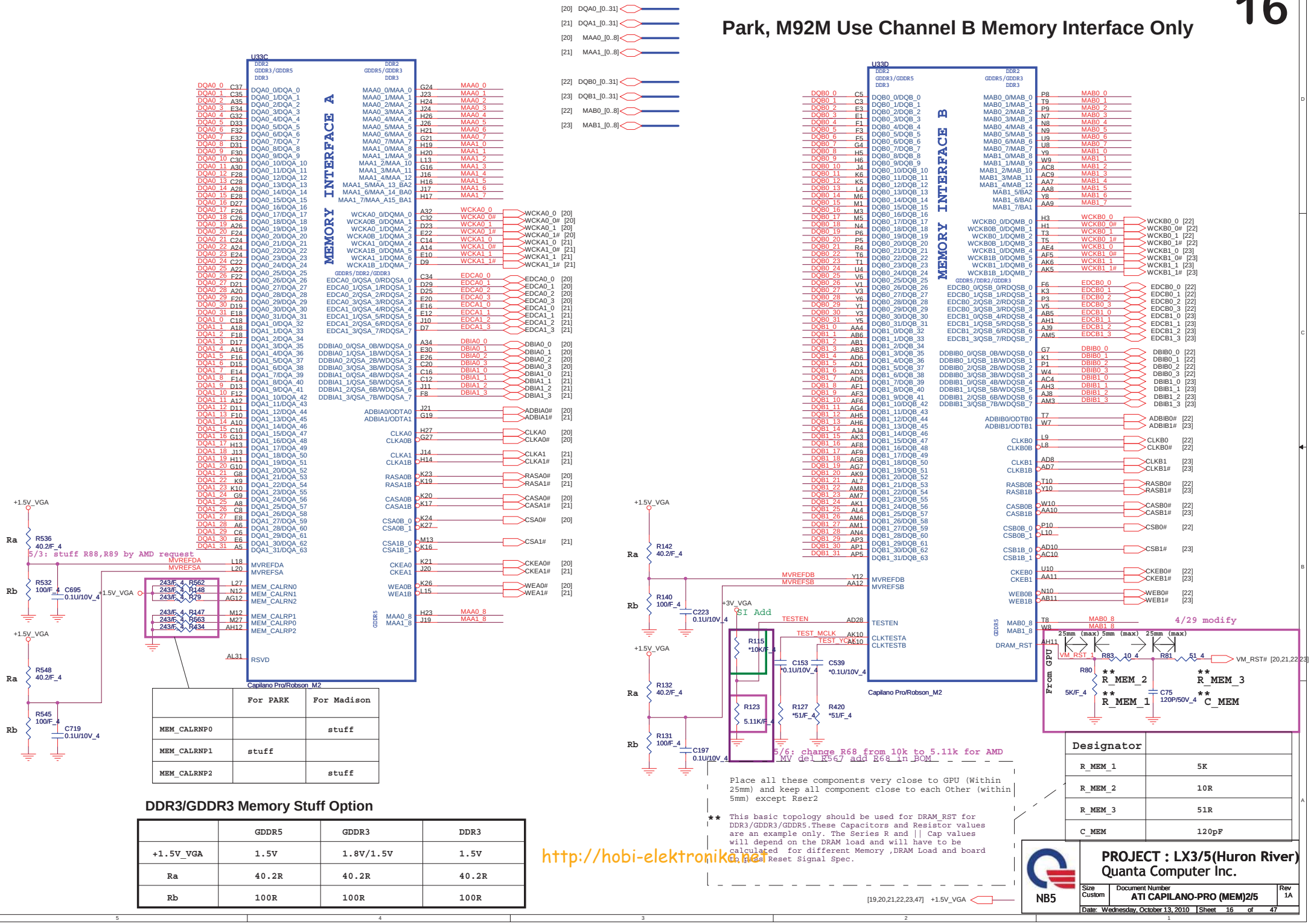
NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CATI APILANO-PRO (MEM)1/5	1A

Date: Wednesday, October 13, 2010 Sheet 15 of 47

Park, M92M Use Channel B Memory Interface Only



	For PARK	For Madison
MEM_CALRNP0		stuff
MEM_CALRNP1	stuff	
MEM_CALRNP2		stuff

DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

Designator	
R_MEM_1	5K
R_MEM_2	10R
R_MEM_3	51R
C_MEM	120pF

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI CAPILANO-PRO (MEM)2/5	1A

Date: Wednesday, October 13, 2010 | Sheet 16 of 47

U33B

MUTI GPU

NC on Park/Robson/Seymour

5/3: modify for GDDR5 table

+1.8V_VGA

R453 *10K/F_4 MEM_ID0
R455 *10K/F_4 MEM_ID1
R448 *10K/F_4 MEM_ID2
R446 *10K/F_4 MEM_ID3

SI Add for AMD request

R77 *10K/F_4 GPIO24_TRSTB
+3V_VGA
R76 *10K/F_4 GPIO27_TMS
TP38 XTALIN R429 *0_4 GPIO26_TCK

MV del in BOM

5/5:add a TP

6/30 :Modify TP

NC on Park/Robson/Seymour

Access to SCL and SDA is mandatory on BACO designs for debug purposes

5/6 add for AMD

+3V_VGA R56 *4.7K_4 R57 *4.7K_4

[24] GPU_EDIDCLK
[24] GPU_EDIDDATA

I2C

SCL
SDA

GPIO0: option to control PSI in future products - not currently qualified

6/11 DB2 modify
8/13 PV modify

R425 0_4

SI-2 Add

4/29 add.

+3V_VGA
R74 *10K/F_4
R109 *10K/F_4

GPU_LVDS_BLON
VGA_GPIO8
VGA_GPIO9
VGA_GPIO10
VGA_GPIO11
VGA_GPIO12
VGA_GPIO13
GPU_PROCHOT

GFX_CORE_CNTRL
VGA_ALERT
TP7

4/29 modify.

GFX_CORE_CNTRL1
VGA_GPIO21_BBEN
VGA_GPIO22

TP5 GPIO24_TRSTB
TP6 GPIO25_TDI
GPIO26_TCK
GPIO27_TMS
TP1
TP4
GPIO28_TDO
GENERICA
TP8
GENERICC

Seymour/Whistler: Stereo sync output
Madison/Capilano: Alternate DP clock source & Stereo sync output

6/30 SI Modify TP GenericF/G is NC on PARK

TMDS_HPD

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

+1.8V_VGA
R78 499/F_4
R117 249/F_4
+VGA_VREFG
C82 0.1U/10V_4

GND Option If XO_IN/XO_IN2 not used
For M97, XO_IN and XO_IN2 should be grounded

+1.8VDPLL_PVDD
+1.0VDPLL_VDDC
CLK_27M
CLK_100M
TP3
TP2

4/20 DB modify.

GFX_THMD
GFX_THMD

+1.8V_TSVDD

GENERAL PURPOSE I/O
PLL/CLOCK
THERMAL

DP Channel D is NC on Park, Robson and Seymour

C918 5.6P/16V_4
C919 5.6P/16V_4
C920 5.6P/16V_4
R482 150/F_4
R480 150/F_4
R477 150/F_4
GPU_CRT_R
GPU_CRT_G
GPU_CRT_B

8/13 PV modify
10/13 PV2 EMI request

GPU_CRT_R [24]
GPU_CRT_G [24]
GPU_CRT_B [24]

VGA STRAPS

GPU_HSYNC [18,24]
GPU_VSYNC [18,24]

R105 499/F_4
DAC1_RSET
+1.8V_AVDD
+VDD1D

Seymour/Whistler: DAC2 is NC
Madison/Capilano: DAC2 can be used for PS2(CRT) output or be left unconnected

Seymour/Whistler: DAC2 is NC
Madison/Capilano:DAC2 Output-C
Madison/Capilano:DAC2 Output-Y

VGA STRAPS

HSYNC_DAC2 [18]
VSYNC_DAC2 [18]

For FL/GL support on Seymour/Whistler only
Seymour/Whistler: GENCLK_CLK
Seymour/Whistler: GENCLK_VSYNC

R476 *0_4/S
R464 *0_4/S
+1.8V_VGA
For future back compatibility

R488 *0_4/S
R465 *0_4/S
+3V_VGA
+1.8V_A2VDDQ

NC on Seymour/Whistler

R129 715/F_4
DAC2_RSET

Seymour/Whistler:TSVSSQ Temperature sensor quiet ground.
Madison/Capilano: A2VSSQ.

DDC1 AND AUX1 CAN BE JOINTED TOGETHER FOR DUAL DCC/AUX FUNCTION
REFER THE DATABOOK FOR DETAIL

DDC2 AND AUX2 CAN BE JOINTED TOGETHER FOR DUAL DCC/AUX FUNCTION
REFER THE DATABOOK FOR DETAIL

DDCxx_AUX3x is NC on M92M2

DDCxx_AUX4x is NC on M92M2 and Park/Robson/Seymour

DDCxx_AUX7x is NC on M9x and Park/Robson/Seymour

GPU_DDCCLK [24]
GPU_DDCDATA [24]

Capilano Pro/Robson_M2

U33G

LVDS CONTROL
LVTMDP

R73 10K_4
R72 10K_4
GPU_DPST_PWM
GPU_DISP_ON

GPU_DPST_PWM [24]
GPU_DISP_ON [24]

GPU_TXUCLKOUT+ [24]
GPU_TXUCLKOUT- [24]
GPU_TXUOUT0+ [24]
GPU_TXUOUT0- [24]
GPU_TXUOUT1+ [24]
GPU_TXUOUT1- [24]
GPU_TXUOUT2+ [24]
GPU_TXUOUT2- [24]
GPU_TXLCLKOUT+ [24]
GPU_TXLCLKOUT- [24]
GPU_TXLOUT0+ [24]
GPU_TXLOUT0- [24]
GPU_TXLOUT1+ [24]
GPU_TXLOUT1- [24]
GPU_TXLOUT2+ [24]
GPU_TXLOUT2- [24]

Capilano Pro/Robson_M2

+1.8V_VGA
L13 HCB1608KF-181T15/1.5A_6 +1.8V_AVDD
(DAC1_AVDD: 1.8V@70mA+42mA)
(A2VDDQ: 1.8V@1mA)
L38 HCB1608KF-181T15/1.5A_6 +1.8V_A2VDDQ
C571 1U/6.3V_4
C579 0.1U/10V_4

+1.8V_VGA
(DAC1_VDD1DI:1.8V@100mA)
L12 HCB1608KF-181T15/1.5A_6 +VDD1D
C141 10U/6.3VS_6
C561 1U/6.3V_4
C560 0.1U/10V_4
SI Add

DPLL_VDCC M97 1.0V/M96 1.1V

+1.8V_VGA
(1.8V@150mA DPLL_PVDD)
L11 HCB1608KF-181T15/1.5A_6 +1.8VDPLL_PVDD
C97 10U/6.3V_8
C107 1U/6.3V_4
C101 0.1U/10V_4

+1.0V_VGA
(1.0V@300mA DPLL_VDDC)
L8 HCB1608KF-181T15/1.5A_6 +1.0VDPLL_VDDC
C73 10U/6.3V_8
C78 1U/6.3V_4
C79 0.1U/10V_4

+1.8V_VGA
(1.8V@20mA TSVDD)
L16 HCB1608KF-181T15/1.5A_6 +1.8V_TSVDD
C114 10U/6.3V_8
C108 1U/6.3V_4

GPIO15	GPIO20	+VGACORE
Low	Low	1.05V
Low	High	1V
High	Low	0.95V
High	High	0.9V

MEM_ID	3	2	1	0	Verona		
DVPDATA	3	2	1	0	GDDR5 Type	Configuration	Size
1	0	0	0	1	Samsung K4G10325FE-HC05 (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
2	0	0	1	0	Hynix H5GQ1H24AFR-T0C BGA (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
3	0	0	1	1			

GPIO6	+VDDCI
High	1.07V
Low	1.12V

[15,19,43] +1.0V_VGA
[15,19,42] +1.8V_VGA
[16,18,19,27,42] +3V_VGA

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size: Custom | Document Number: ATI CAPILANO-PRO DISPLAY3/5 | Rev: 1A

Date: Wednesday, October 13, 2010 | Sheet 17 of 47

U33F

GND

Capilano Pro/Robson_M2

STRAPS

+3V_VGA

[17] VGA_GPIO0 R107 10K/F_4
[17] VGA_GPIO1 R110 10K/F_4
[17] VGA_GPIO2 R405 *10K/F_4
[17] VGA_GPIO8 R381 *10K/F_4
[17] VGA_GPIO9 R75 *10K/F_4

5/6: Add pu down for GPIO table

[17] VGA_GPIO13 R396 *10K/F_4, R406 10K/F_4
[17] VGA_GPIO12 R61 10K/F_4, R69 *10K/F_4
[17] VGA_GPIO11 R410 *10K/F_4, R409 10K/F_4
[17] VGA_GPIO10 R392 *10K/F_4

add GPIO10 for EEPROM 4/23.

[17] GENERICC R66 *10K/F_4
[17] VGA_GPIO22 R393 10K/F_4

5/6: Add for Enable EEPROM

[17,24] GPU_VSYNC R484 10K/F_4
[17,24] GPU_HSYNC R489 10K/F_4

[17] VSYNC_DAC2 R119 *10K/F_4
[17] HSYNC_DAC2 R118 *10K/F_4

[17,24] GPU_LVDS_BLON R343 10K/F_4
[17,42] GFX_CORE_CNTRL0 R378 3K/F_4
[17,42] GFX_CORE_CNTRL1 R379 3K/F_4

5/10 add pu down by AMD request.

Table 3-34 ROM Configurations

Manufacturer	Part Number	Size	CONFIG[2:0]
Atmel	AT25F512	512 kbit	001
	AT25F512A	512 kbit	010
	AT25F1024	1 Mbit	011
	AT25F1024A	1 Mbit	011
	AT25F2048	2 Mbit	011
	AT25F4096	4 Mbit	011
ST Microelectronics	M25P05A	512 kbit	100
	M25P10A	1 Mbit	101
	M25P20	2 Mbit	101
	M25P40	4 Mbit	101
	M25P80	8 Mbit	101
Silicon Storage Technology	SST25VF512	512 kbit	010
	SST25VF010	1 Mbit	011
	SST25VF020	2 Mbit	011
	SST25VF040	4 Mbit	011
Winbond Electronics Corporation	W45B512	512 kbit	110
	W45B012	1 Mbit	111
YMC	Y25LF05	512 kbit	010
	SA25C020	2 Mbit	011
PMC	Pm25LV512	512 kbit	100
	Pm25LV010	1 Mbit	101

Default

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set t 0.

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

27MHz + 100Mhz OSC Option

5/10 modify

4/29 reserve PCH_CLK

6/23: SI modify

+3V

C551 12P/50V_4 — TP60 — Y3 27MHZ — TP61 — C543 12P/50V_4
R444 1M/F_4
R457 *0_4/S

[9] PCH_CLK_27M — *0_4 R461

+3V_VGA
L7 HCB1608KF-181T15_6
L4 *HCB1608KF-181T15_6
C537 .1U/10V_4
C556 .1U/10V_4

U28 SL16010DCT
XTALIN XTALOUT
VDD_100M VDD_27M 100M_OUT
SS_SEL0 SS_SEL1 27M_OUT
GND_100M GND_27M GND_PAD

SS_SEL0 SS_SEL1

CLK_100M_R — CLK_27M_R

R442 10K/F_4 R437 *10K/F_4
SS_SEL0 SS_SEL1
R451 10K/F_4 R452 10K/F_4

R449 *0_4/S — GENERICA [17]
R445 *0_4/S — CLK_100M [17]
R433 *0_4/S — GPIO26_TCK [17]
R435 *0_4/S — CLK_27M [17]

C546 10P/50V_4 C530 10P/50V_4

Reserve for support BACO mode

PX_EN_1 — R91 *0_4/S — R92 *0_4 — PX_EN [19]

For PX_EN, refer to the BACO reference schematics for detail

For GDDR5 EEPROM

+3V_VGA

4/20 DB update

R383 10K/F_4

[17] VGA_GPIO22 R384 33_4
[17] VGA_GPIO10 R367 33_4
[17] VGA_GPIO9 R368 33_4
[17] VGA_GPIO8 R385 33_4

U22
CE# SCK SI SO WP# VDD HOLD# VSS

+3V_VGA — R387 10K/F_4 — TP62 TP63

C490 0.1U/10V_4

6/23: SI modify

Thermal Sensor

4/19: change only from VGA

[35] GPUT_CLK — R419 *0_4/S — G_SMBCLK [17]
[35] GPUT_DATA — R428 *0_4/S — G_SMBDAT [17]

+3V_VGA
R68 4.7K_4
R67 4.7K_4
R64 10K_4

U6
SMCLK SMDATA -ALT GND VCC DXP DXN -OVT
*G781-1P8@EV

[17,35] VGA_ALERT — VGA_ALERT R423 *0_4/S

781-1_3V R54 *200/F_6 — +3V_VGA
C50 *0.1U/10V_4
GFX_THMD+ — GFX_THMD+ [17]
C527 *2200P/50V_4
GFX_THMD- — GFX_THMD- [17]
-VGATHRM R63 *10K_4 — +3V_VGA

I2C ADDRESS: 9AH

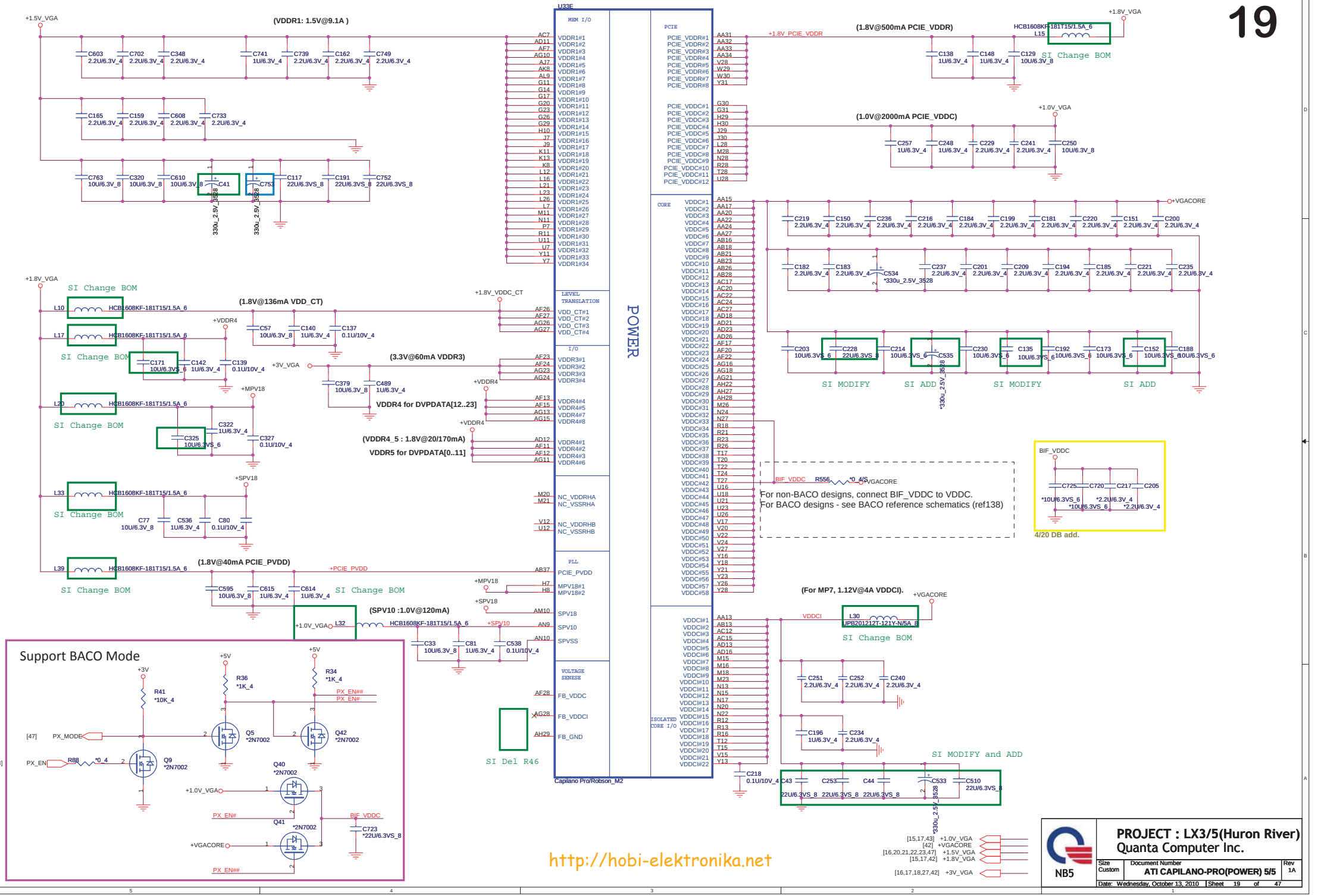
w/s 10 / 10

[16,17,19,27,42] +3V_VGA

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

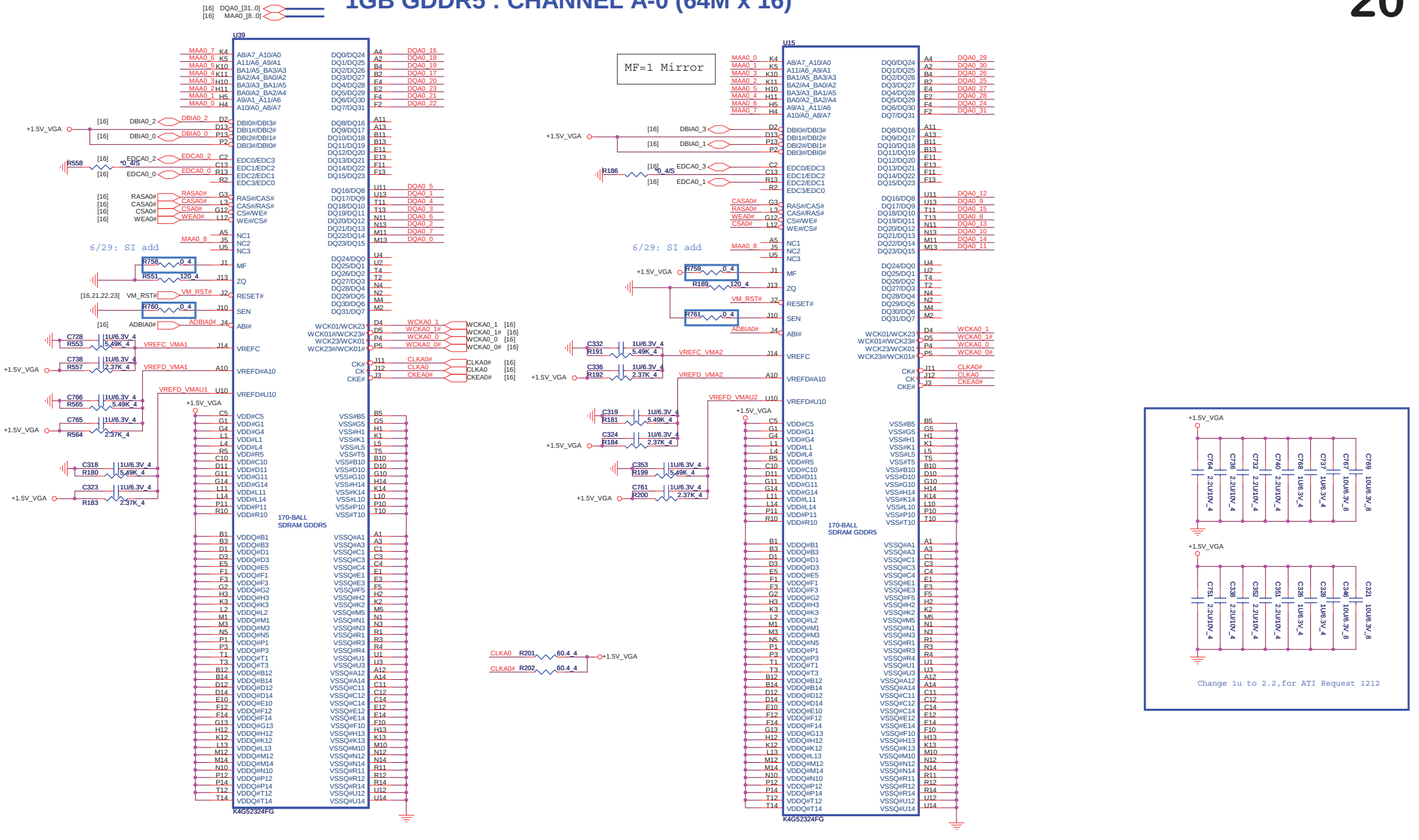
Size	Document Number	Rev
Custom	ATI CAPILANO-PRO(GD&Str)4/5	1A
Date: Wednesday, October 13, 2010	Sheet 18 of 47	



PROJECT :	LX3/5(Huron River)
	Quanta Computer Inc.
Size: Custom	Document Number: ATI CAPILANO-PRO(POWER) 5/5
Rev: 1A	
Date: Wednesday, October 13, 2010	Sheet 19 of 47

NB5

1GB GDDR5 : CHANNEL A-0 (64M x 16)



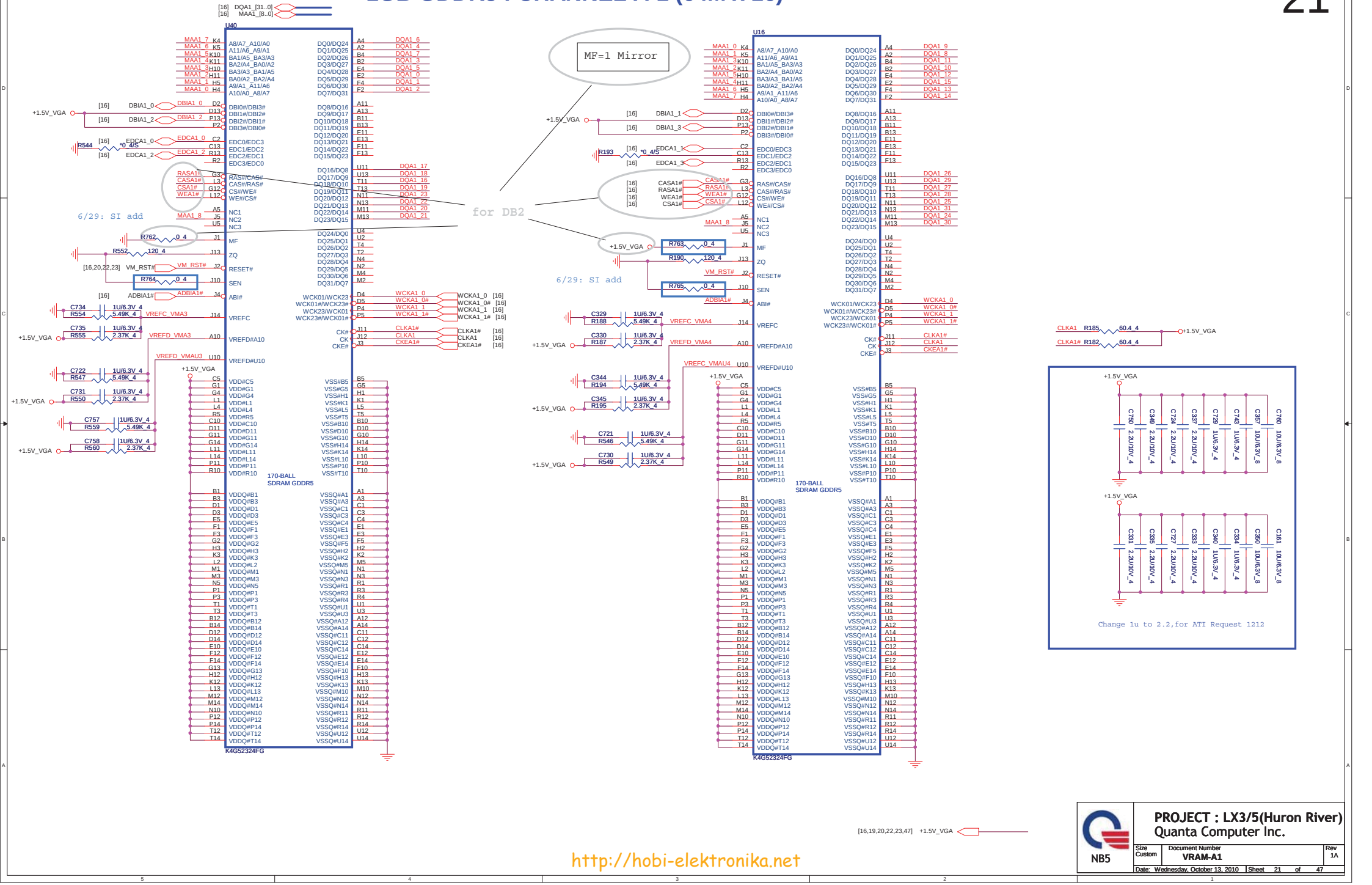
NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VRAM-A0	1A

Date: Wednesday, October 13, 2010 | Sheet 20 of 47

1GB GDDR5 : CHANNEL A-1 (64M x 16)



PROJECT :	LX3/5(Huron River)
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: VRAM-A1; Rev: 1A
Date: Wednesday, October 13, 2010	Sheet 21 of 47

1GB GDDR5 : CHANNEL B-0 (64M x 16)

[16] DQB0_[0..31]
[16] MAB0_[0..8]

U12

MAB0_7 K4
MAB0_6 K5
MAB0_5 K10
MAB0_4 K11
MAB0_3 H10
MAB0_2 H11
MAB0_1 H5
MAB0_0 H4

A8/A7_A10/A0
A11/A6_A9/A1
BA1/A5_BA3/A3
BA2/A4_BA0/A2
BA3/A3_BA1/A5
BA0/A2_BA2/A4
A9/A1_A11/A6
A10/A0_A8/A7

DBIB0_2 D2
DBIB0_0 P13
P2

DBI0#/DBI3#
DBI1#/DBI2#
DBI2#/DBI1#
DBI3#/DBI0#

EDCB0_2 C2
EDCB0_0 R13
R2

EDC0/EDC3
EDC1/EDC2
EDC2/EDC1
EDC3/EDC0

RASB0# G3
CASB0# L3
CSB0# G12
WEB0# L12

RAS#/CAS#
CAS#/RAS#
CS#/WE#
WE#/CS#

MAB0_8 A5 J5 U5

NC1
NC2
NC3

6/29: SI add

R767 0_4 J1
R167 120_4 J13

MF
ZQ

VM_RST# J2
RESET#

R769 0_4 J10
SEN

ADBIB0# J4
ABI#

C285 1U/6.3V_4
R168 5.49K_4
VREFC_VMB1 J14
VREFC

C281 1U/6.3V_4
R169 2.37K_4
VREFD_VMB1 A10
VREFD#A10

C284 1U/6.3V_4
R165 5.49K_4
C283 1U/6.3V_4
R171 2.37K_4
VREFD_VMBU1 U10
VREFD#U10

C267 1U/6.3V_4
R155 5.49K_4
C249 1U/6.3V_4
R150 2.37K_4

+1.5V_VGA

VDD#C5 C5
VDD#G1 G1
VDD#G4 G4
VDD#L1 L1
VDD#L4 L4
VDD#R5 R5
VDD#C10 C10
VDD#D11 D11
VDD#G11 G11
VDD#G14 G14
VDD#L11 L11
VDD#L14 L14
VDD#P11 P11
VDD#R10 R10

VDDQ#B1 B1
VDDQ#B3 B3
VDDQ#D1 D1
VDDQ#D3 D3
VDDQ#E5 E5
VDDQ#F1 F1
VDDQ#F3 F3
VDDQ#G2 G2
VDDQ#H3 H3
VDDQ#K3 K3
VDDQ#L2 L2
VDDQ#M1 M1
VDDQ#M3 M3
VDDQ#N5 N5
VDDQ#P1 P1
VDDQ#P3 P3
VDDQ#T1 T1
VDDQ#T3 T3
VDDQ#B12 B12
VDDQ#B14 B14
VDDQ#D12 D12
VDDQ#D14 D14
VDDQ#E10 E10
VDDQ#F12 F12
VDDQ#F14 F14
VDDQ#G13 G13
VDDQ#H12 H12
VDDQ#K12 K12
VDDQ#L13 L13
VDDQ#M12 M12
VDDQ#M14 M14
VDDQ#N10 N10
VDDQ#P12 P12
VDDQ#P14 P14
VDDQ#T12 T12
VDDQ#T14 T14

170-BALL SDRAM GDDR5

VSS#B5 B5
VSS#G5 G5
VSS#H1 H1
VSS#K1 K1
VSS#L5 L5
VSS#T5 T5
VSS#B10 B10
VSS#D10 D10
VSS#G10 G10
VSS#H14 H14
VSS#K14 K14
VSS#L10 L10
VSS#P10 P10
VSS#T10 T10

VSSQ#A1 A1
VSSQ#A3 A3
VSSQ#C1 C1
VSSQ#C3 C3
VSSQ#C4 C4
VSSQ#E1 E1
VSSQ#E3 E3
VSSQ#F5 F5
VSSQ#H2 H2
VSSQ#K2 K2
VSSQ#M5 M5
VSSQ#N1 N1
VSSQ#N3 N3
VSSQ#R1 R1
VSSQ#R3 R3
VSSQ#R4 R4
VSSQ#U1 U1
VSSQ#U3 U3
VSSQ#A12 A12
VSSQ#A14 A14
VSSQ#C11 C11
VSSQ#C12 C12
VSSQ#C14 C14
VSSQ#E12 E12
VSSQ#E14 E14
VSSQ#F10 F10
VSSQ#H13 H13
VSSQ#K13 K13
VSSQ#M10 M10
VSSQ#N12 N12
VSSQ#N14 N14
VSSQ#R11 R11
VSSQ#R12 R12
VSSQ#R14 R14
VSSQ#U12 U12
VSSQ#U14 U14

K4G52324FG

DQ0/DQ24 A4 DQB0_21
DQ1/DQ25 A2 DQB0_18
DQ2/DQ26 B4 DQB0_20
DQ3/DQ27 B2 DQB0_16
DQ4/DQ28 E4 DQB0_19
DQ5/DQ29 E2 DQB0_23
DQ6/DQ30 F4 DQB0_17
DQ7/DQ31 F2 DQB0_22

DQ8/DQ16 A11
DQ9/DQ17 A13
DQ10/DQ18 B11
DQ11/DQ19 B13
DQ12/DQ20 E11
DQ13/DQ21 E13
DQ14/DQ22 F11
DQ15/DQ23 F13

DQ16/DQ8 U11 DQB0_2
DQ17/DQ9 U13 DQB0_1
DQ18/DQ10 T11 DQB0_3
DQ19/DQ11 T13 DQB0_0
DQ20/DQ12 N11 DQB0_6
DQ21/DQ13 N13 DQB0_5
DQ22/DQ14 M11 DQB0_7
DQ23/DQ15 M13 DQB0_4

DQ24/DQ0 U4
DQ25/DQ1 U2
DQ26/DQ2 T4
DQ27/DQ3 T2
DQ28/DQ4 N4
DQ29/DQ5 N2
DQ30/DQ6 M4
DQ31/DQ7 M2

WCK01/WCK23 D4 WCKB0_1
WCK01#/WCK23# D5 WCKB0_1# [16]
WCK23/WCK01 P4 WCKB0_0 [16]
WCK23#/WCK01# P5 WCKB0_0# [16]

CK# J11 CLKB0# [16]
CK J12 CLKB0 [16]
CKE# J3 CKEB0# [16]

MF=1 Mirror

U36

MAB0_0 K4
MAB0_1 K5
MAB0_3 K10
MAB0_2 K11
MAB0_5 H10
MAB0_4 H11
MAB0_6 H5
MAB0_7 H4

A8/A7_A10/A0
A11/A6_A9/A1
BA1/A5_BA3/A3
BA2/A4_BA0/A2
BA3/A3_BA1/A5
BA0/A2_BA2/A4
A9/A1_A11/A6
A10/A0_A8/A7

DBIB0_3 D2
DBIB0_1 P13
P2

DBI0#/DBI3#
DBI1#/DBI2#
DBI2#/DBI1#
DBI3#/DBI0#

EDCB0_3 C2
EDCB0_1 R13
R2

EDC0/EDC3
EDC1/EDC2
EDC2/EDC1
EDC3/EDC0

CASB0# G3
RASB0# L3
WEB0# G12
CSB0# L12

RAS#/CAS#
CAS#/RAS#
CS#/WE#
WE#/CS#

MAB0_8 A5 J5 U5

NC1
NC2
NC3

6/29: SI add

R766 0_4 J1
R539 120_4 J13

MF
ZQ

VM_RST# J2
RESET#

R768 0_4 J10
SEN

ADBIB0# J4
ABI#

C703 1U/6.3V_4
R540 5.49K_4
VREFC_VMB2 J14
VREFC

C711 1U/6.3V_4
R538 2.37K_4
VREFD_VMB2 A10
VREFD#A10

C691 1U/6.3V_4
R530 5.49K_4
C698 1U/6.3V_4
R537 2.37K_4
VREFD_VMBU2 U10
VREFD#U10

C282 1U/6.3V_4
R174 5.49K_4
C286 1U/6.3V_4
R173 2.37K_4

+1.5V_VGA

VDD#C5 C5
VDD#G1 G1
VDD#G4 G4
VDD#L1 L1
VDD#L4 L4
VDD#R5 R5
VDD#C10 C10
VDD#D11 D11
VDD#G11 G11
VDD#G14 G14
VDD#L11 L11
VDD#L14 L14
VDD#P11 P11
VDD#R10 R10

VDDQ#B1 B1
VDDQ#B3 B3
VDDQ#D1 D1
VDDQ#D3 D3
VDDQ#E5 E5
VDDQ#F1 F1
VDDQ#F3 F3
VDDQ#G2 G2
VDDQ#H3 H3
VDDQ#K3 K3
VDDQ#L2 L2
VDDQ#M1 M1
VDDQ#M3 M3
VDDQ#N5 N5
VDDQ#P1 P1
VDDQ#P3 P3
VDDQ#T1 T1
VDDQ#T3 T3
VDDQ#B12 B12
VDDQ#B14 B14
VDDQ#D12 D12
VDDQ#D14 D14
VDDQ#E10 E10
VDDQ#F12 F12
VDDQ#F14 F14
VDDQ#G13 G13
VDDQ#H12 H12
VDDQ#K12 K12
VDDQ#L13 L13
VDDQ#M12 M12
VDDQ#M14 M14
VDDQ#N10 N10
VDDQ#P12 P12
VDDQ#P14 P14
VDDQ#T12 T12
VDDQ#T14 T14

170-BALL SDRAM GDDR5

VSS#B5 B5
VSS#G5 G5
VSS#H1 H1
VSS#K1 K1
VSS#L5 L5
VSS#T5 T5
VSS#B10 B10
VSS#D10 D10
VSS#G10 G10
VSS#H14 H14
VSS#K14 K14
VSS#L10 L10
VSS#P10 P10
VSS#T10 T10

VSSQ#A1 A1
VSSQ#A3 A3
VSSQ#C1 C1
VSSQ#C3 C3
VSSQ#C4 C4
VSSQ#E1 E1
VSSQ#E3 E3
VSSQ#F5 F5
VSSQ#H2 H2
VSSQ#K2 K2
VSSQ#M5 M5
VSSQ#N1 N1
VSSQ#N3 N3
VSSQ#R1 R1
VSSQ#R3 R3
VSSQ#R4 R4
VSSQ#U1 U1
VSSQ#U3 U3
VSSQ#A12 A12
VSSQ#A14 A14
VSSQ#C11 C11
VSSQ#C12 C12
VSSQ#C14 C14
VSSQ#E12 E12
VSSQ#E14 E14
VSSQ#F10 F10
VSSQ#H13 H13
VSSQ#K13 K13
VSSQ#M10 M10
VSSQ#N12 N12
VSSQ#N14 N14
VSSQ#R11 R11
VSSQ#R12 R12
VSSQ#R14 R14
VSSQ#U12 U12
VSSQ#U14 U14

K4G52324FG

DQ0/DQ24 A4 DQB0_24
DQ1/DQ25 A2 DQB0_25
DQ2/DQ26 B4 DQB0_27
DQ3/DQ27 B2 DQB0_28
DQ4/DQ28 E4 DQB0_31
DQ5/DQ29 E2 DQB0_30
DQ6/DQ30 F4 DQB0_26
DQ7/DQ31 F2 DQB0_29

DQ8/DQ16 A11
DQ9/DQ17 A13
DQ10/DQ18 B11
DQ11/DQ19 B13
DQ12/DQ20 E11
DQ13/DQ21 E13
DQ14/DQ22 F11
DQ15/DQ23 F13

DQ16/DQ8 U11 DQB0_13
DQ17/DQ9 U13 DQB0_10
DQ18/DQ10 T11 DQB0_11
DQ19/DQ11 T13 DQB0_12
DQ20/DQ12 N11 DQB0_15
DQ21/DQ13 N13 DQB0_8
DQ22/DQ14 M11 DQB0_14
DQ23/DQ15 M13 DQB0_9

DQ24/DQ0 U4
DQ25/DQ1 U2
DQ26/DQ2 T4
DQ27/DQ3 T2
DQ28/DQ4 N4
DQ29/DQ5 N2
DQ30/DQ6 M4
DQ31/DQ7 M2

WCK01/WCK23 D4 WCKB0_1
WCK01#/WCK23# D5 WCKB0_1#
WCK23/WCK01 P4 WCKB0_0
WCK23#/WCK01# P5 WCKB0_0#

CK# J11 CLKB0#
CK J12 CLKB0
CKE# J3 CKEB0#

CLKB0 R159 60.4_4
CLKB0# R163 60.4_4

+1.5V_VGA

+1.5V_VGA
C709 2.2U/10V_4
C602 2.2U/10V_4
C601 2.2U/10V_4
C607 2.2U/10V_4
C522 1U/6.3V_4
C167 1U/6.3V_4
C667 10U/6.3V_8
C604 10U/6.3V_8

+1.5V_VGA
C605 2.2U/10V_4
C611 2.2U/10V_4
C609 2.2U/10V_4
C48 2.2U/10V_4
C160 1U/6.3V_4
C158 1U/6.3V_4
C280 10U/6.3V_8
C606 10U/6.3V_8

Change 1u to 2.2,for ATI Request 1212

+1.5V_VGA [16,19,20,21,23,47]

[16,19,20,21,23,47] +1.5V_VGA

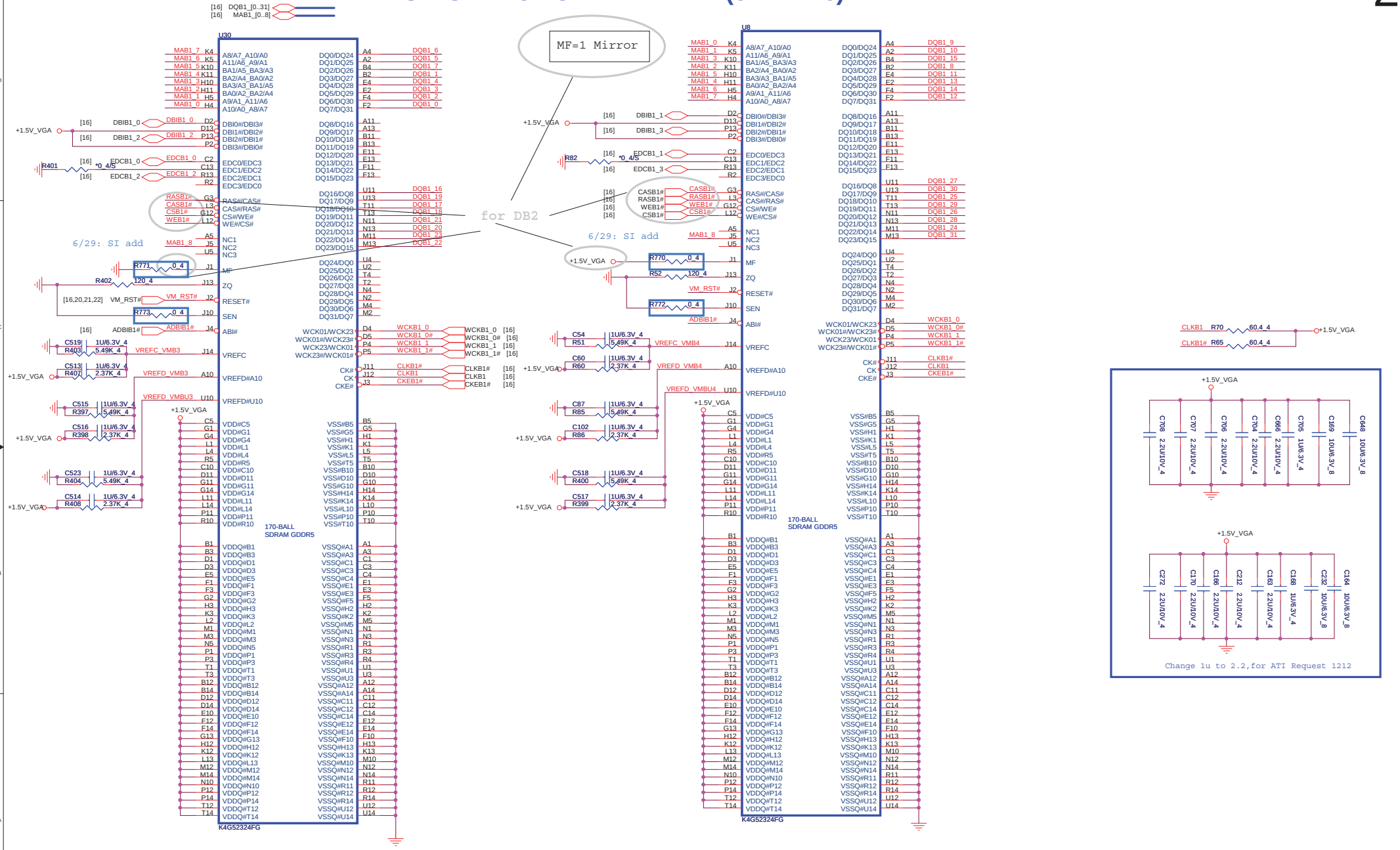
NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VRAM-B0	1A

Date: Wednesday, October 13, 2010 Sheet 22 of 47

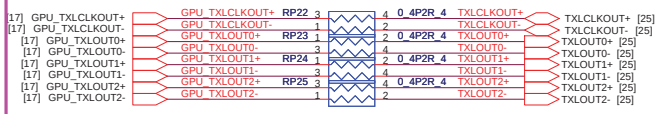
1GB GDDR5 : CHANNEL B-1 (64M x 16)



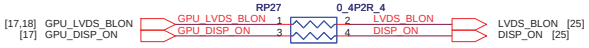
PROJECT :	LX3/5(Huron River)
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: VRAM-B1
Rev: 1A	
Date: Wednesday, October 13, 2010	Sheet 23 of 47

FOR DIS ONLY

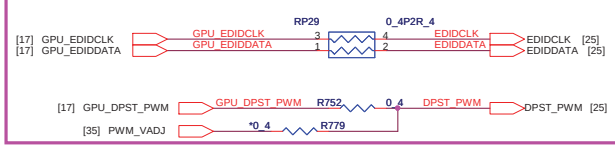
OPTION SIGNAL FROM NB to LVDS for DIS



OPTION Back Light SIGNAL FROM NB to LVDS for DIS

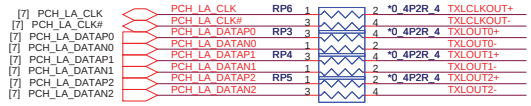


OPTION SIGNAL FROM NB to LVDS for DIS

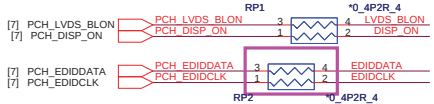


FOR UMA ONLY

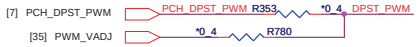
OPTION SIGNAL FROM NB to LVDS for UMA



OPTION Back Light SIGNAL FROM NB to LVDS for UMA

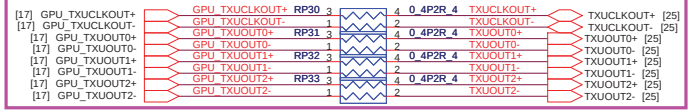


OPTION SIGNAL FROM NB to LVDS for UMA

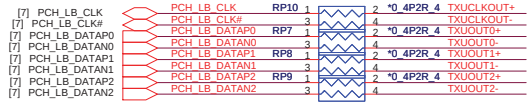


FOR UMA/SG

FOR 17"DIS ONLY

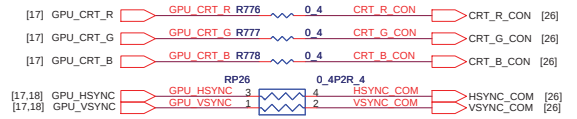


FOR 17"UMA ONLY

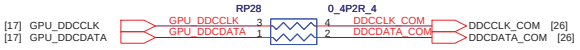


FOR DIS ONLY

OPTION SIGNAL FROM NB to CRT for DIS

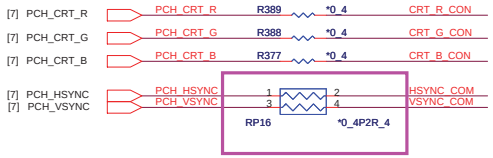


OPTION SIGNAL FROM NB to CRT for DIS



FOR UMA ONLY

OPTION SIGNAL FROM NB to CRT for UMA



5/11:for Layout modify

OPTION SIGNAL FROM NB to CRT for UMA

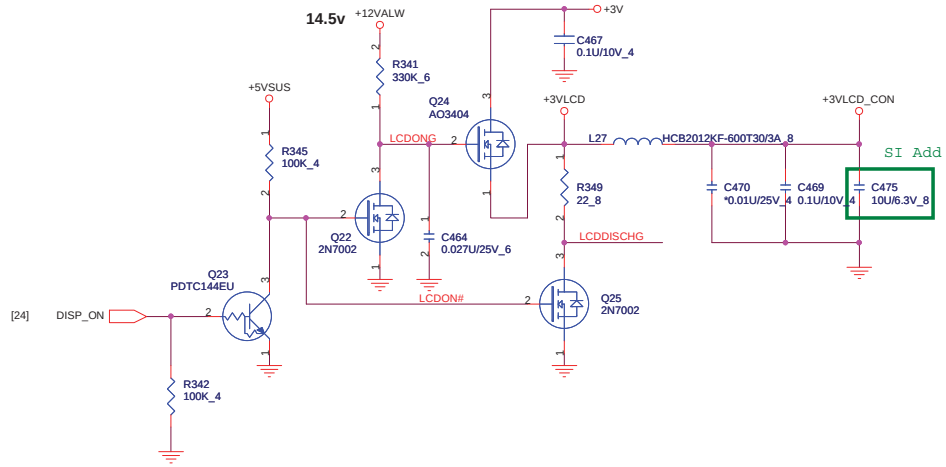
9/26 :MV Modify

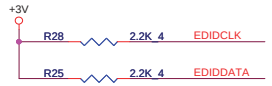
+3V [3,7,8,9,10,11,13,14,18,19,25,26,27,28,29,30,31,32,33,34,35,36,37,39,40,41,43,45,46,47]
+5V [7,8,11,19,25,26,27,29,30,32,34,36,37,45]
+1.8V [5,8,11,39,45]

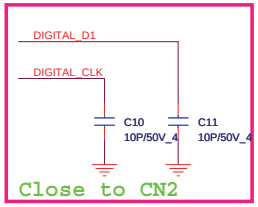
NB5

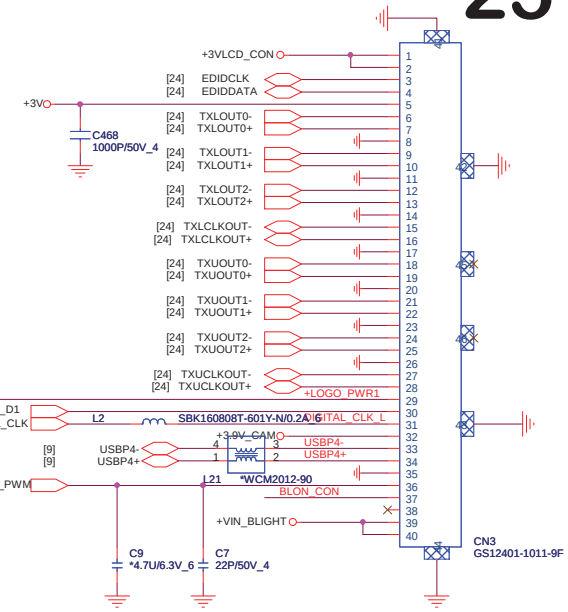
PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

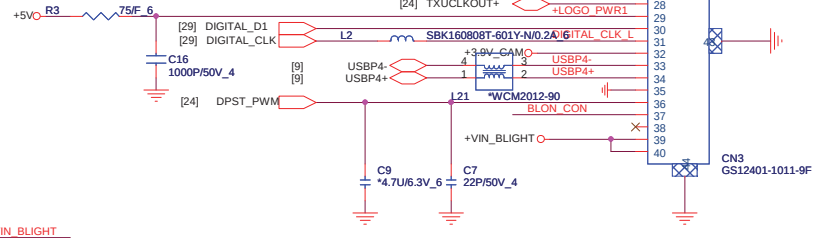
Size	Document Number	Rev
Custom	SWITCHABLE	1A
Date: Wednesday, October 13, 2010	Sheet 24 of 47	

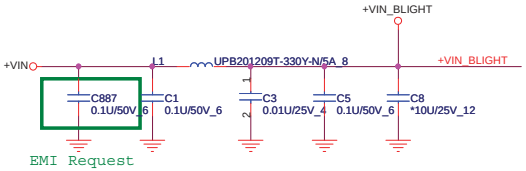


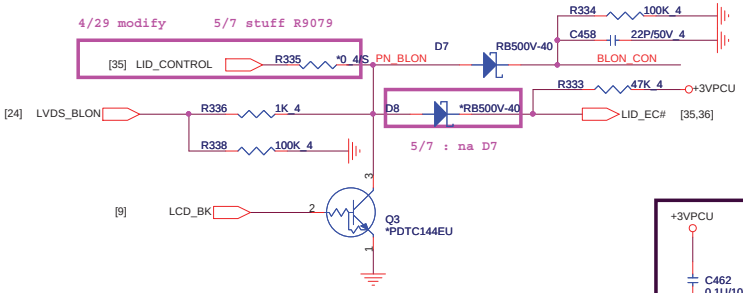


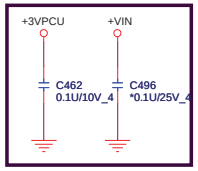


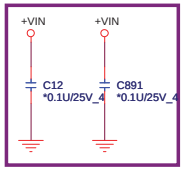


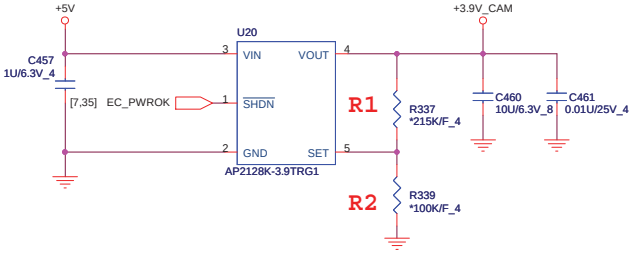












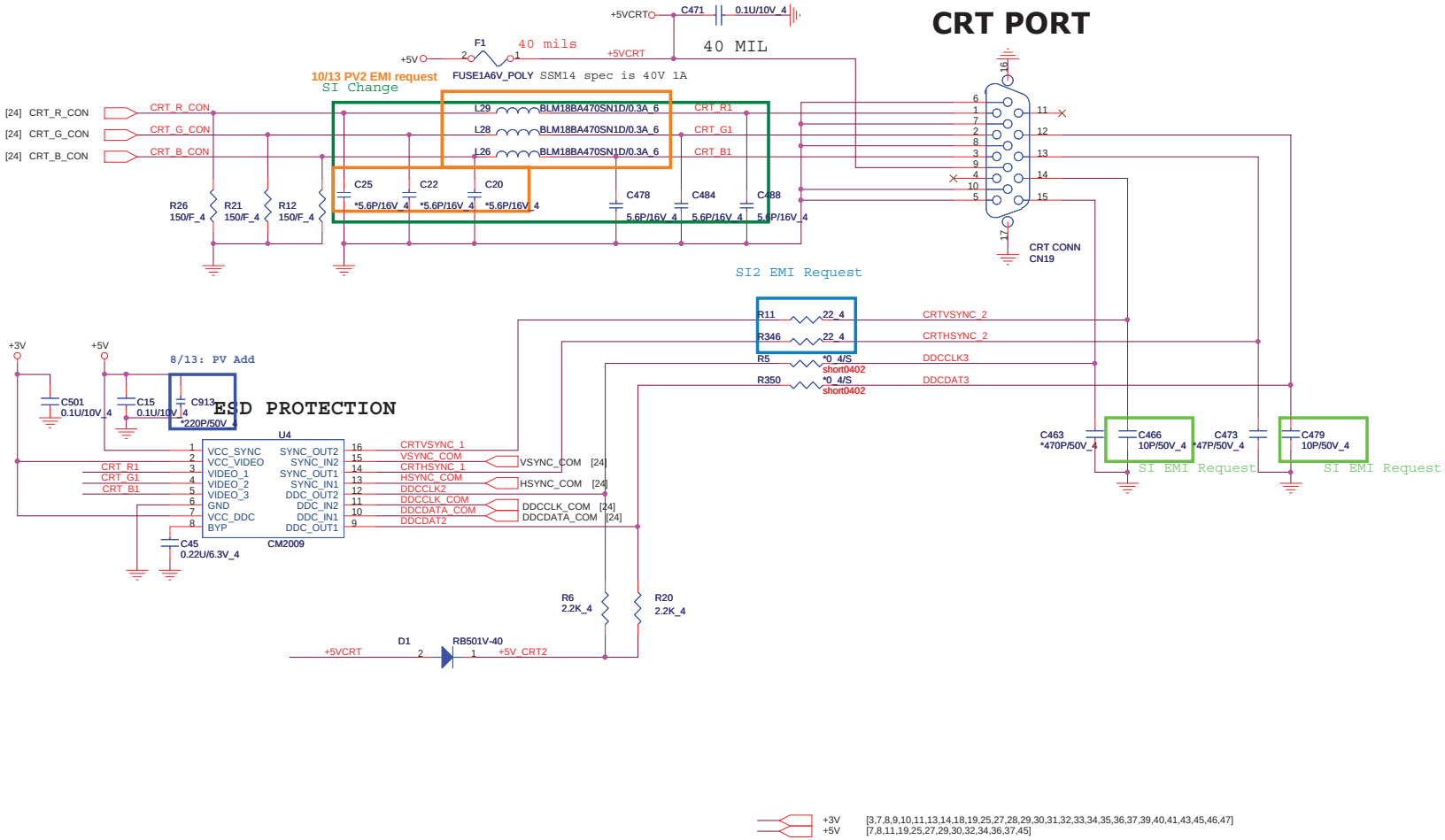
[3,7,8,9,10,11,13,14,18,19,26,27,28,29,30,31,32,33,34,35,36,37,39,40,41,43,45,46,47] +3V
[7,8,11,19,26,27,29,30,32,34,36,37,45] +5V
[31,38,39,41,42,43,44,45] +VIN
[7,8,32,34,35,36,37,38,39,40,42,44,45,47] +3VPCU
[34,37,42,44,45] +12VALW

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID function	1A
Date: Wednesday, October 13, 2010	Sheet 25 of 47	

CRT PORT



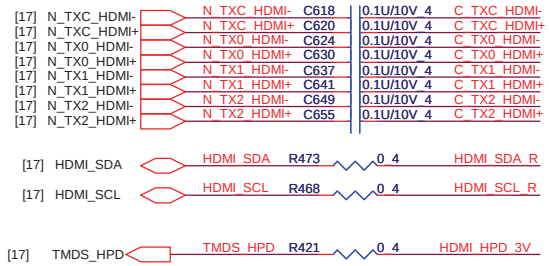
NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

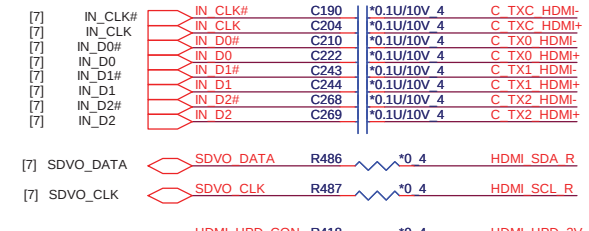
Size	Document Number	Rev
Custom	CRT/HDMI Conn	1A

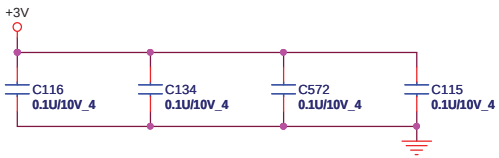
Date: Wednesday, October 13, 2010 Sheet 26 of 47

DIS/SG HDMI



UMA ONLY HDMI

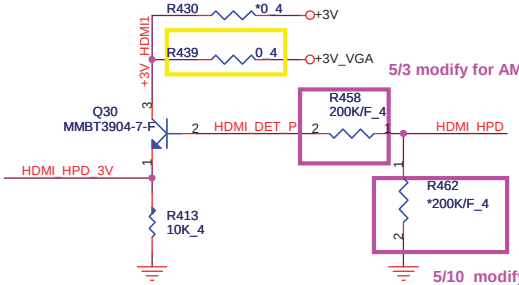


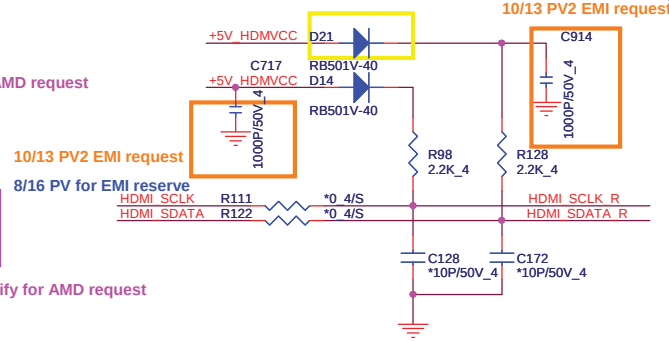


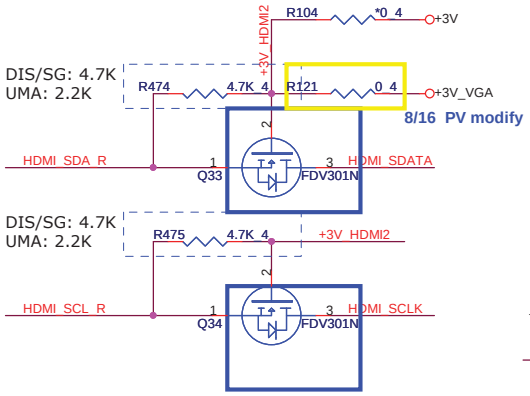
HDMI CON_COM

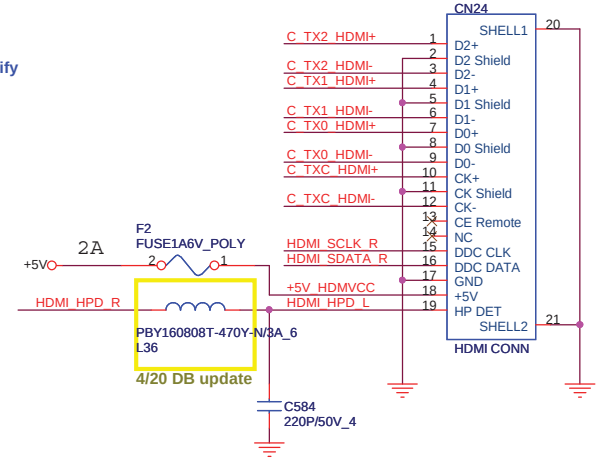
27

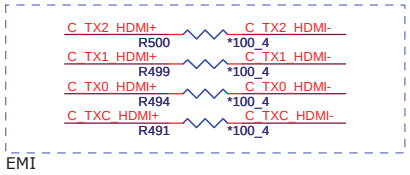
9/26: MV Del C906,C914
9/26: MV Add D21

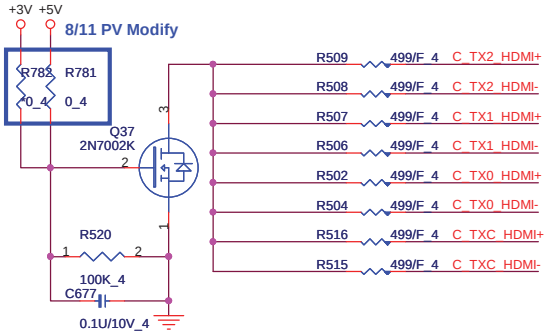


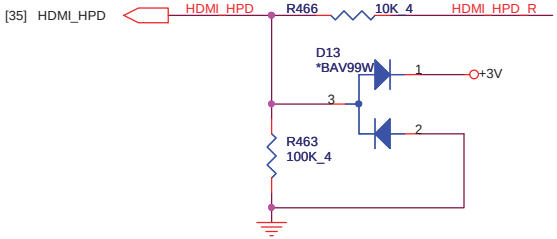










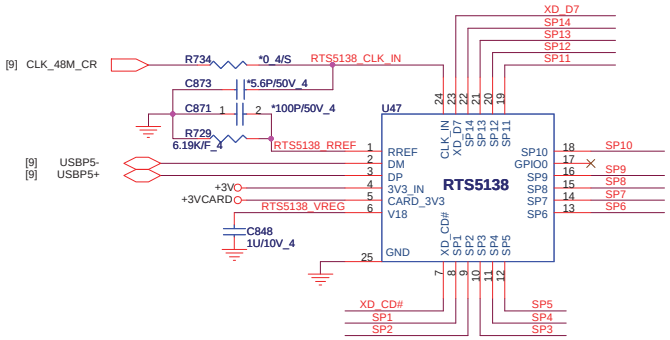


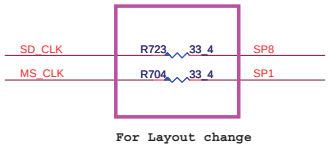
NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/POWER CONN	1A

Date: Wednesday, October 13, 2010 Sheet 27 of 47

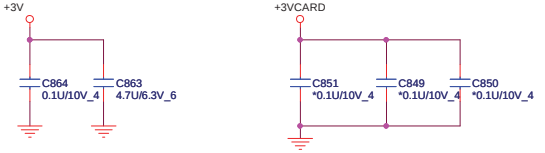




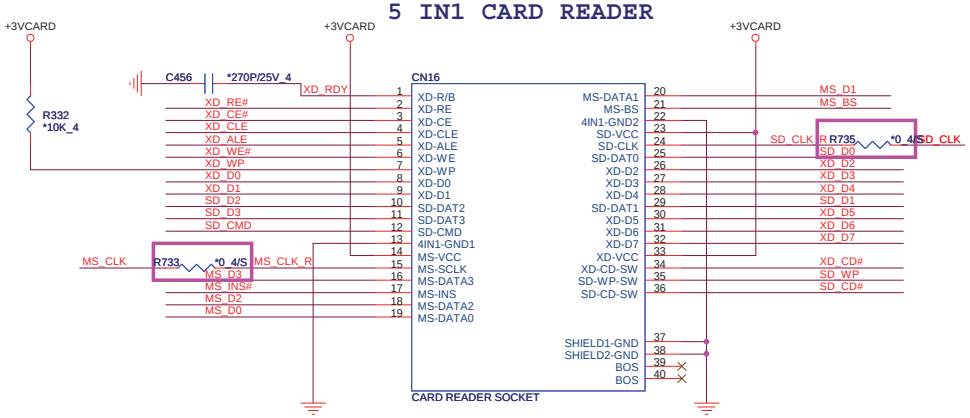
For Layout change

	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	
SP14	XD_D6		MS_BS
	XD_D7		

Share Pin



XD,MMC/SD,MS/MSP 5 IN1 CARD READER



5 IN1 CARD-READER (PUSH-PUSH)

Support SD/SD PRO/MMC/MS/MS PRO/xD Cards

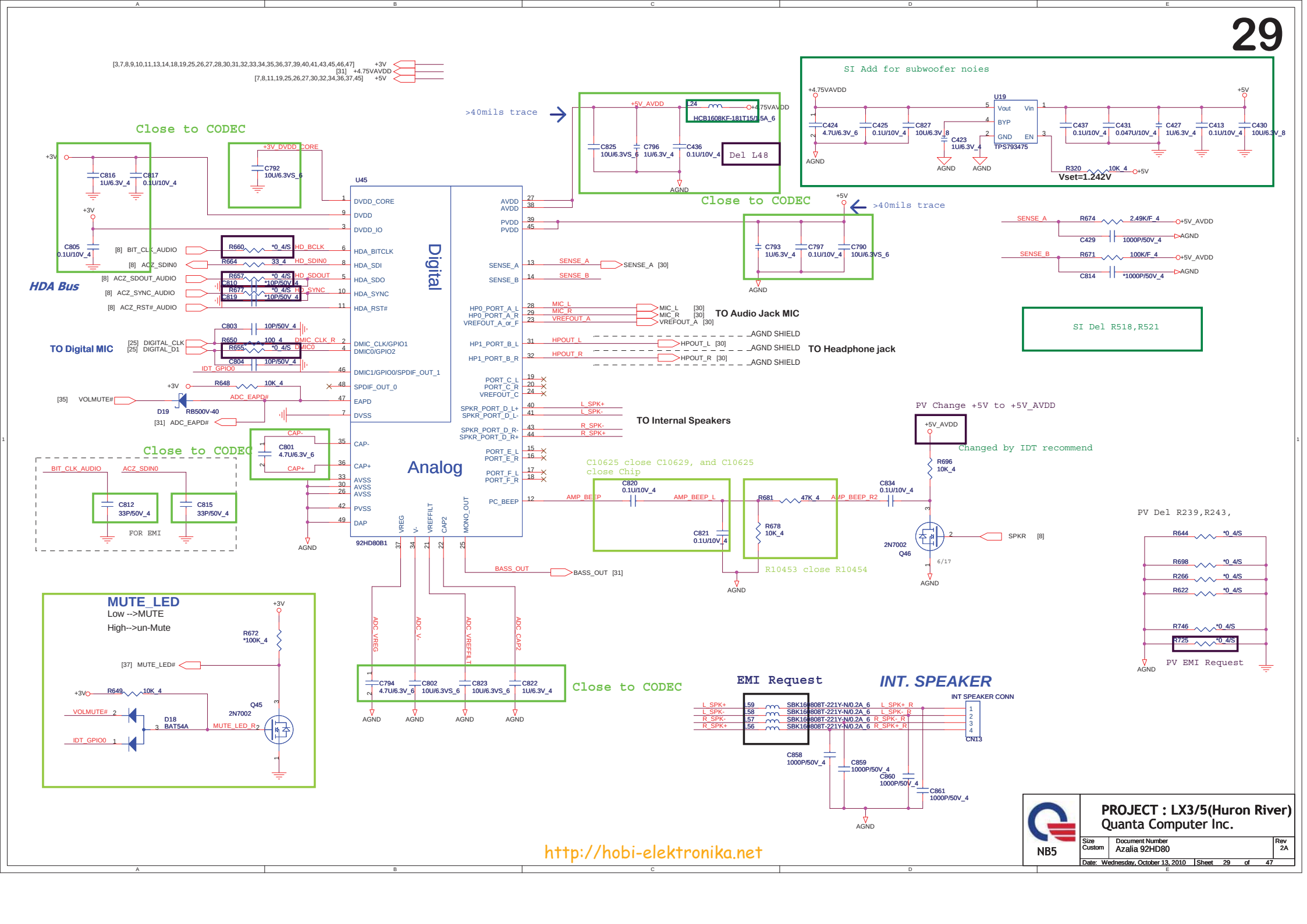
+3V [3,7,8,9,10,11,13,14,18,19,25,26,27,29,30,31,32,33,34,35,36,37,39,40,41,43,45,46,47]

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5138 & CR SOCKET	1A

Date: Wednesday, October 13, 2010 Sheet 28 of 47


[3,7,8,9,10,11,13,14,18,19,25,26,27,28,30,31,32,33,34,35,36,37,39,40,41,43,45,46,47] +3V
[31] +4.75VAVDD
[7,8,11,19,25,26,27,30,32,34,36,37,45] +5V
SI Add for subwoofer noies
+4.75VAVDD
U19
Vout Vin
BYP
GND EN
TPS793475
C424 4.7U/6.3V_6
C425 0.1U/10V_4
C827 10U/6.3V_8
C423 1U/6.3V_4
C437 0.1U/10V_4
C431 0.047U/10V_4
C427 1U/6.3V_4
C413 0.1U/10V_4
C430 10U/6.3V_8
R320 10K_4
Vset=1.242V
>40mils trace
+5V_AVDD
HCB1608KF-181T15/1.5A_6
C825 10U/6.3VS_6
C796 1U/6.3V_4
C436 0.1U/10V_4
Del L48
Close to CODEC
Close to CODEC
>40mils trace
C793 1U/6.3V_4
C797 0.1U/10V_4
C790 10U/6.3VS_6
SENSE_A R674 2.49K/F_4 +5V_AVDD
C429 1000P/50V_4 AGND
SENSE_B R671 100K/F_4 +5V_AVDD
C814 *1000P/50V_4 AGND
SI Del R518,R521
Close to CODEC
C816 1U/6.3V_4
C817 0.1U/10V_4
C792 10U/6.3VS_6
+3V_DVDD_CORE
U45
Digital
DVDD_CORE
DVDD
DVDD_IO
HDA_BITCLK
HDA_SDI
HDA_SDO
HDA_SYNC
HDA_RST#
C805 0.1U/10V_4
[8] BIT_CLK_AUDIO
[8] ACZ_SDIN0
[8] ACZ_SDOUT_AUDIO
[8] ACZ_SYNC_AUDIO
[8] ACZ_RST#_AUDIO
R660 *0_4/S HD_BCLK
R664 33_4 HD_SDIN0
R657 *0_4/S HD_SDOUT
C810 *10P/50V_4
R677 *0_4/S HD_SYNC
C819 *10P/50V_4
HDA Bus
TO Digital MIC
C803 10P/50V_4
R650 100_4 DMIC_CLK_R
R655 *0_4/S DMIC0
C804 10P/50V_4
IDT_GPIO0
[25] DIGITAL_CLK
[25] DIGITAL_D1
DMIC_CLK/GPIO1
DMIC0/GPIO2
DMIC1/GPIO0/SPDIF_OUT_1
SPDIF_OUT_0
EAPD
DVSS
R648 10K_4
ADC_EAPD#
[35] VOLMUTE#
D19 RB500V-40
[31] ADC_EAPD#
Close to CODEC
C801 4.7U/6.3V_6
CAP-
CAP+
CAP-
CAP+
AVSS
AVSS
AVSS
PVSS
DAP
BIT_CLK_AUDIO
ACZ_SDIN0
C812 33P/50V_4
C815 33P/50V_4
FOR EMI
AGND
Analog
92HD80B1
VREG
V-
VREFFILT
CAP2
MONO_OUT
AVDD
AVDD
PVDD
PVDD
SENSE_A
SENSE_B
SENSE_A [30]
HP0_PORT_A_L
HP0_PORT_A_R
VREFOUT_A_or_F
MIC_L
MIC_R
VREFOUT_A
MIC_L [30]
MIC_R [30]
VREFOUT_A [30]
TO Audio Jack MIC
HP1_PORT_B_L
HP1_PORT_B_R
HPOUT_L
HPOUT_R
HPOUT_L [30]
HPOUT_R [30]
AGND SHIELD
AGND SHIELD
AGND SHIELD
TO Headphone jack
PORT_C_L
PORT_C_R
VREFOUT_C
SPKR_PORT_D_L+
SPKR_PORT_D_L-
SPKR_PORT_D_R-
SPKR_PORT_D_R+
L_SPK+
L_SPK-
R_SPK-
R_SPK+
TO Internal Speakers
PORT_E_L
PORT_E_R
PORT_F_L
PORT_F_R
PC_BEEP
BASS_OUT
BASS_OUT [31]
C10625 close C10629, and C10625 close Chip
C820 0.1U/10V_4
AMP_BEEP
AMP_BEEP_L
C821 0.1U/10V_4
R681 47K_4
AMP_BEEP_R2
R678 10K_4
R10453 close R10454
PV Change +5V to +5V_AVDD
+5V_AVDD
Changed by IDT recommend
R696 10K_4
C834 0.1U/10V_4
2N7002 Q46
SPKR [8]
6/17
AGND
PV Del R239,R243,
R644 *0_4/S
R698 *0_4/S
R266 *0_4/S
R622 *0_4/S
R746 *0_4/S
R725 *0_4/S
PV EMI Request
MUTE_LED
Low -->MUTE
High-->un-Mute
R672 *100K_4
[37] MUTE_LED#
R649 10K_4
Q45 2N7002
D18 BAT54A
VOLMUTE#
IDT_GPIO0
MUTE_LED_R
ADC_VREG
ADC_V-
ADC_VREFFILT
ADC_CAP2
C794 4.7U/6.3V_6
C802 10U/6.3VS_6
C823 10U/6.3VS_6
C822 1U/6.3V_4
Close to CODEC
EMI Request
INT. SPEAKER
INT SPEAKER CONN
L_SPK+ L59 SBK160808T-221Y-N/0.2A_6 L_SPK+_R
L_SPK- L58 SBK160808T-221Y-N/0.2A_6 L_SPK-_R
R_SPK- L57 SBK160808T-221Y-N/0.2A_6 R_SPK-_R
R_SPK+ L56 SBK160808T-221Y-N/0.2A_6 R_SPK+_R
CN13
C858 1000P/50V_4
C859 1000P/50V_4
C860 1000P/50V_4
C861 1000P/50V_4
AGND
http://hobi-elektronika.net
NB5
PROJECT : LX3/5(Huron River)
Quanta Computer Inc.
Size Custom
Document Number Azalia 92HD80
Rev 2A
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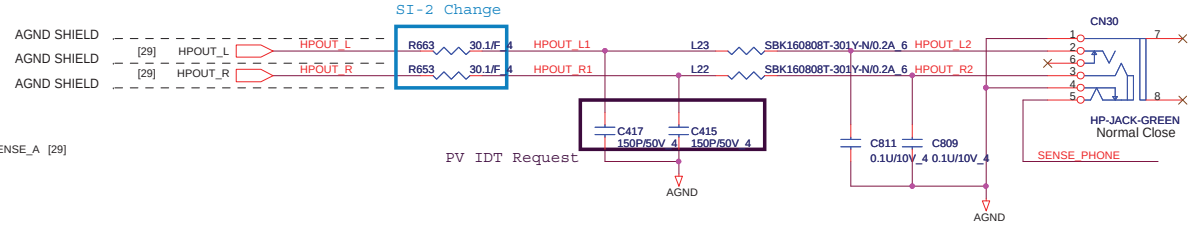
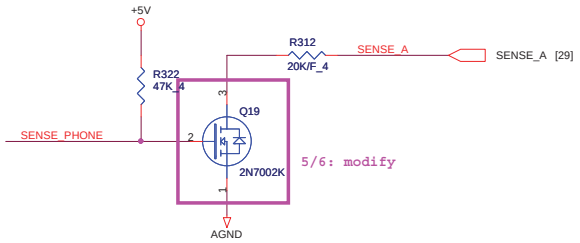
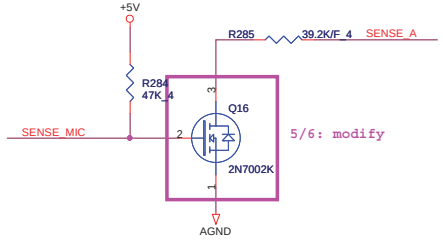
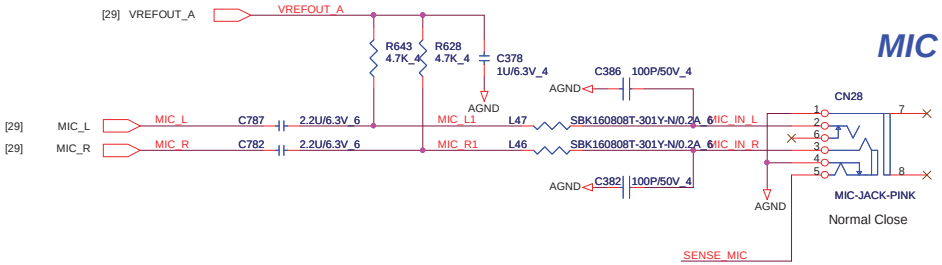
Line out





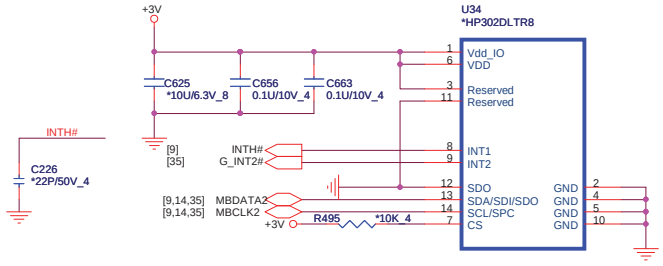


MIC

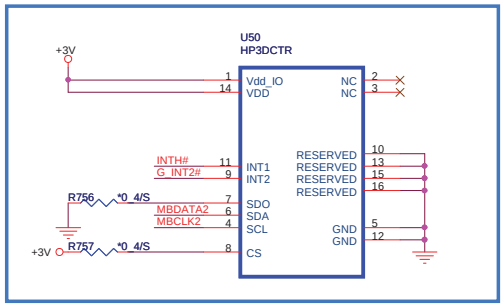


SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low

Accelerometer Sensor



6/23: SI Add

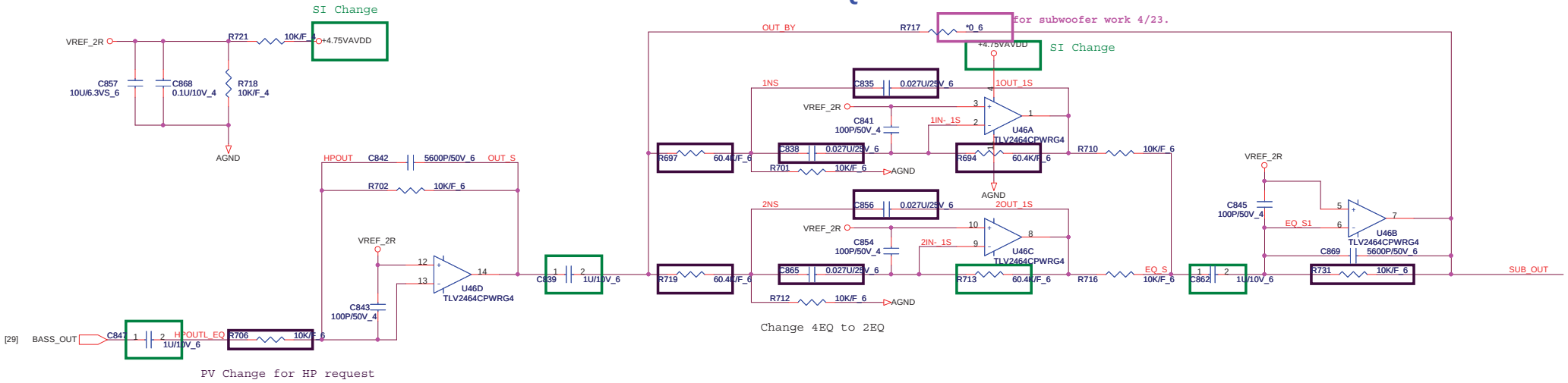


Pin 12: Low 38hex

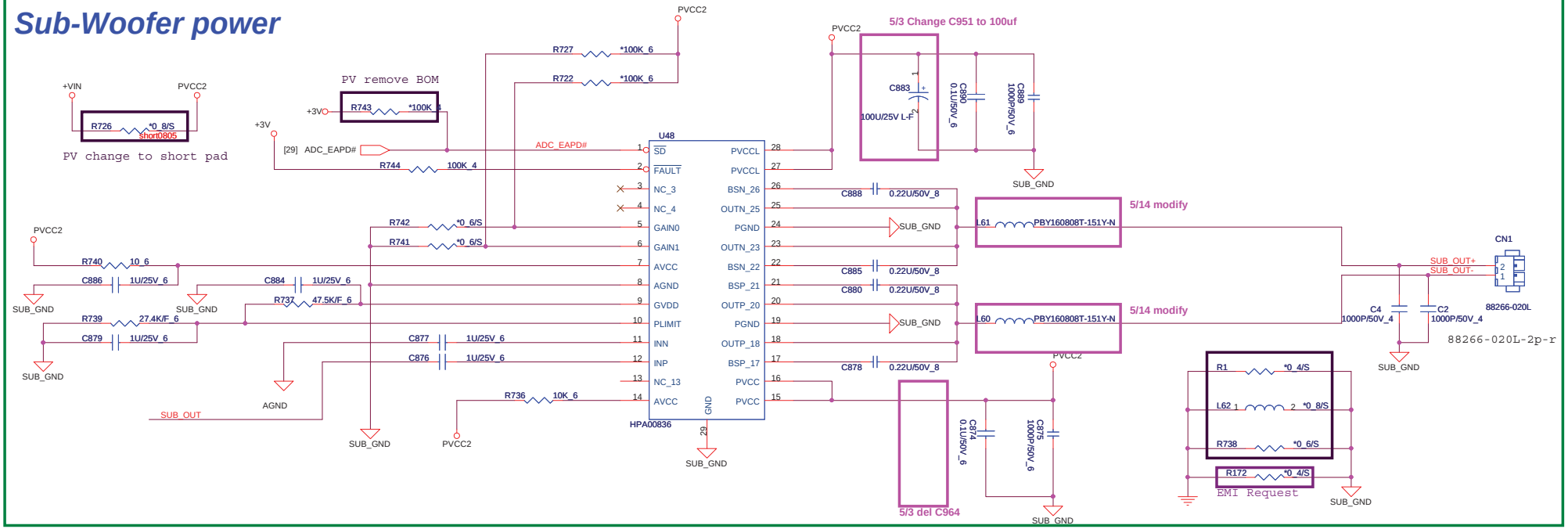
Pin 12: unconnected/floating 3Ahex

NB5	PROJECT : LX3/5(Huron River) Quanta Computer Inc.	
Size: Custom	Document Number: Audio Jack/Accelerometer	Rev: 1A
Date: Wednesday, October 13, 2010	Sheet 30 of 47	

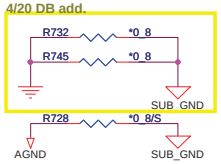
EQ FOR SUBWOOFER



Sub-Woofer power



4/20 DB add.



GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

+3V [3,7,8,9,10,11,13,14,18,19,25,26,27,28,29,30,32,33,34,35,36,37,39,40,41,43,44]
+4.75VAVDD [29]
+VIN [25,38,39,41,42,43,44,45]

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SUBWOOFER (EQ & AMP.)	1A

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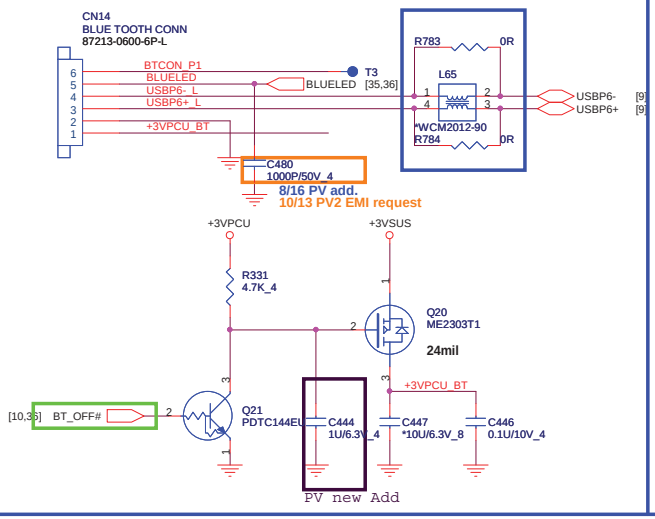
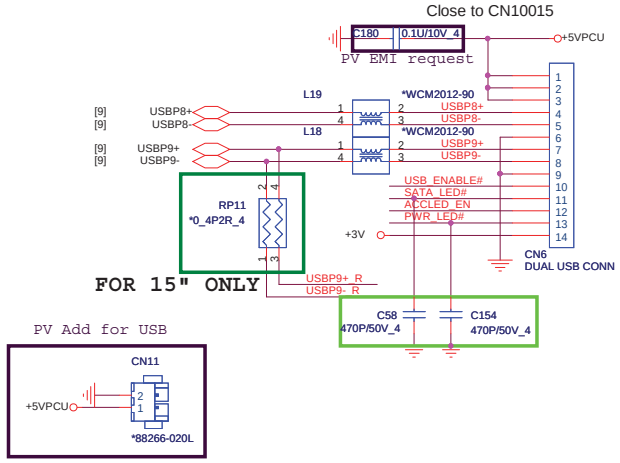
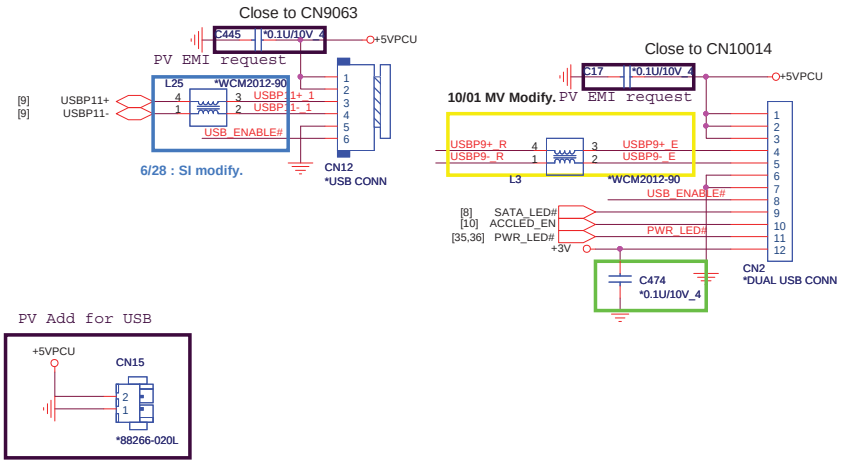
BLUETOOTH



RIGHT SIDE USBX2 for 17"

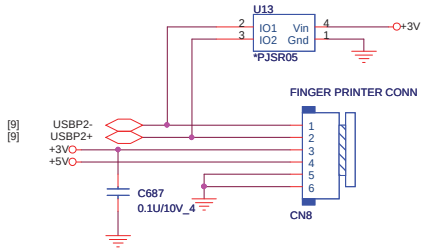


RIGHT SIDE USB for 15"

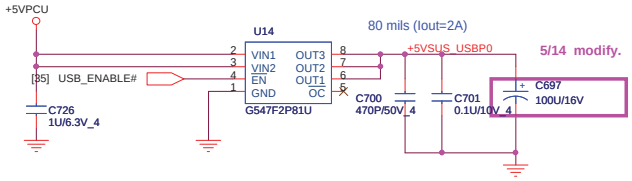


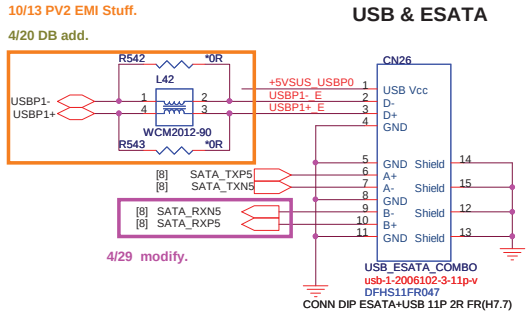
USB fingerprint CON

1. USBP2-
2. USBP2+
3. +3V
4. +5V
5. SYSTEM GND
6. SYSTEM GND

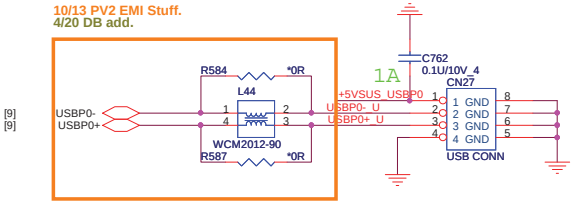


E-SATA

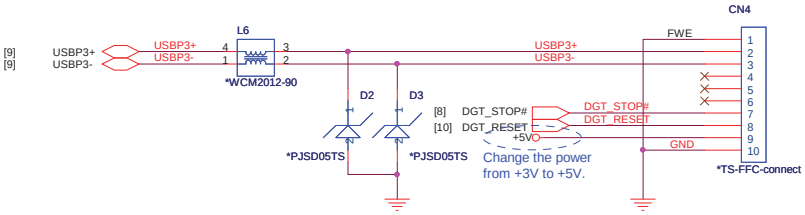




LEFT USB PORT



Touch screen for 15"



NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/WC/FT/Touchscreen	1A
Date: Wednesday, October 13, 2010	Sheet 32 of 47	

For EMI 0 ~ 22 ohm

LAN_XTAL1 — R203 10_4 — XTAL1

Y1 25MHz

XTAL2

C359 33P/50V_4

C354 33P/50V_4

9/29: Modify footprint

+3VLANVCC

C341 0.1U/10V_4 C361 0.1U/10V_4 C343 0.1U/10V_4 C339 0.1U/10V_4

+3V_LAN

C776 22U/6.3VS_8 C364 0.1U/10V_4

Close to Pin 35/34

4/23 modify AL08111DB00 RTL8111DL-GR 4/23 modify

U38 NS892405

C746 *0_4S V_DAC0 MDI0+ MDI0-

C747 *0_4S V_DAC1 MDI1+ MDI1-

C742 *0_4S V_DAC2 MDI2+ MDI2-

C745 *0_4S V_DAC3 MDI3+ MDI3-

C744 0.01U/25V_4

4/29 modify

TCT1 TD1+ TD1- TCT2 TD2+ TD2- TCT3 TD3+ TD3- TCT4 TD4+ TD4-

MCT1 MX1+ MX1- MCT2 MX2+ MX2- MCT3 MX3+ MX3- MCT4 MX4+ MX4-

LAN_MCT0 C290 *0_4S R176 75_4

LAN_MX0+ LAN_MX0-

LAN_MCT1 C287 *0_4S R177 75_4

LAN_MX1+ LAN_MX1-

LAN_MCT2 C288 *0_4S R178 75_4

LAN_MX2+ LAN_MX2-

LAN_MCT3 C289 *0_4S R179 75_4

LAN_MX3+ LAN_MX3-

LAN_MCTG

C718 10P/3KV_1808

10/13 PV2 EMI Request

GND VIA x 9 Pcs

R196 2.49K/F_4 LANRSET

+3V_LAN

+1.05V_LAN +3V_LAN +1.05V_LAN

LAN_TX# LAN_GPIOS R211 1K/F_4 +3V_LAN LAN_GLINK100#

U17 RTL8111E-VB-GR

GND AVDD33 AVDD33(NC) RSET AVDD1 CKXTAL2 CKXTAL1 AVDD3(AVDD1) VDD1(NC) LED3 VDD3 GPO/SMBALERT LED1/EESK

MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- MDI3+ MDI3-

MDIP0 MDIN0 AVDD1(NC) MDIP1 MDIN1 AVDD1(NC) MDIP2(NC) MDIN2(NC) AVDD1(NC) MDIP3(NC) MDIN3(NC) AVDD3(NC)

SROUT1 VDDSR VDDSR ENSR EED/SDA LED3/EDO EECS/SCL DVDD1 LANWAKEB VDD3 ISOLATEB PERSTP

+1.05V_LAN_O +3V_LAN

LAN_GLINK10# R235 10K/F_4 +3V_LAN

LAN_ECS_SCL R585 10K/F_4

+1.05V_LAN PCIE_WAKE# PCIE_WAKE# [7,36]

+3V_LAN ISOLATEB PLTRST# PLTRST# [3,9,35,36,37]

DVDD1 SMBCLK(NC) SMBDATA(NC) CLKREQB HSIP HSIN REFCLK_P REFCLK_M ESD01 HSOP HSON GNDTX

+1.05V_LAN

R197 10K/F_4 LAN_SMBDAT

[9] PCIE_CLKREQ_LAN# PCIE_CLKREQ_LAN# R561 *0_4S LAN_CLKRQ

[9] PCIE_TXP2_LAN PCIE_TXP2_LAN

[9] PCIE_TXN2_LAN PCIE_TXN2_LAN

[9] CLK_PCIE_LANP CLK_PCIE_LANP

[9] CLK_PCIE_LANN CLK_PCIE_LANN

PCIE_RXN2_LAN_L C358 0.1U/10V_4 PCIE_RXN2_LAN [9]

PCIE_RXP2_LAN_L C355 0.1U/10V_4 PCIE_RXP2_LAN [9]

+1.05V_LAN

+3V

R605 1K_4

ISOLATEB R586 *100_4 LAN_DISABLE# [10]

R593 15K/F_4

*RB501V-40 D15

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

IND SMD 4.7UH +-20% 680MA(CBC2518T4R7M)
CV-4707MZ00

Power trace Layout 寬度> 60mil

>60mil

+1.05V_LAN_O L43 CBC2518T4R7M >60mil +1.05V_LAN

Trace<30 mil
Width > 60 mil

C759 0.1U/10V_4

C756 4.7U/6.3V_6

C754 0.1U/10V_4 C342 0.1U/10V_4 C369 0.1U/10V_4 C755 0.1U/10V_4

LAN_GLINK100# LAN_GLED#

LAN_TX# LAN_YLED#

Link

C370 *1000P/50V_4 C356 *1000P/50V_4

+1.05V_LAN

C367 0.1U/10V_4 C748 0.1U/10V_4 C347 0.1U/10V_4 C771 0.1U/10V_4

4/23 modify

Close to Pin 21

RJ45

4/23 modify

+3V_LAN R438 330_4 C550 1000P/50V_4

CN22

LAN_YLED LAN_YLED# LED_GRE_P LED_GRE_N

LAN_MX3+ LAN_MX3- LAN_MX2- LAN_MX1- LAN_MX1+ LAN_MX2+ LAN_MX0+ LAN_MX0-

RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+ GND1 GND

FOR EMI

+3V_LAN R395 330_4 LAN_GLED LAN_GLED# LED_YEL_P LED_YEL_N

C507 1000P/50V_4

RJ45_CONN

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL 8111EL/RJ45	1A

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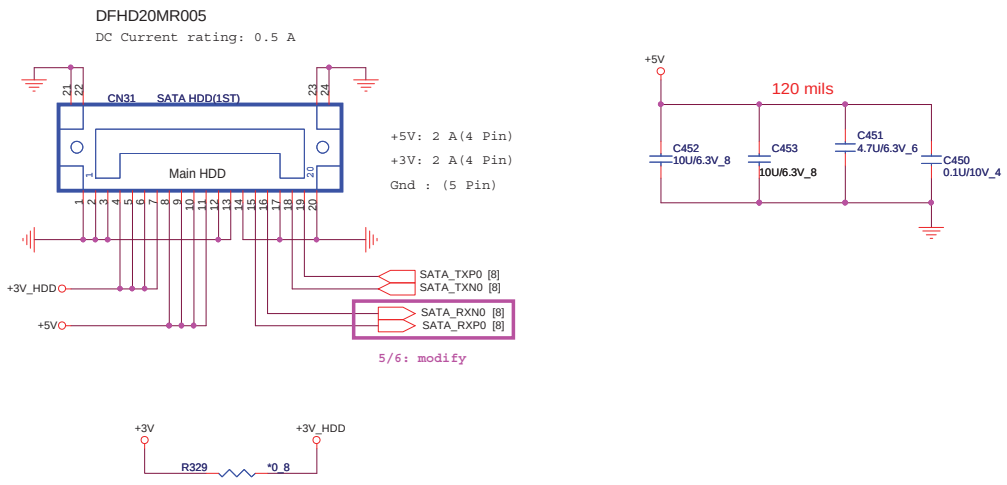
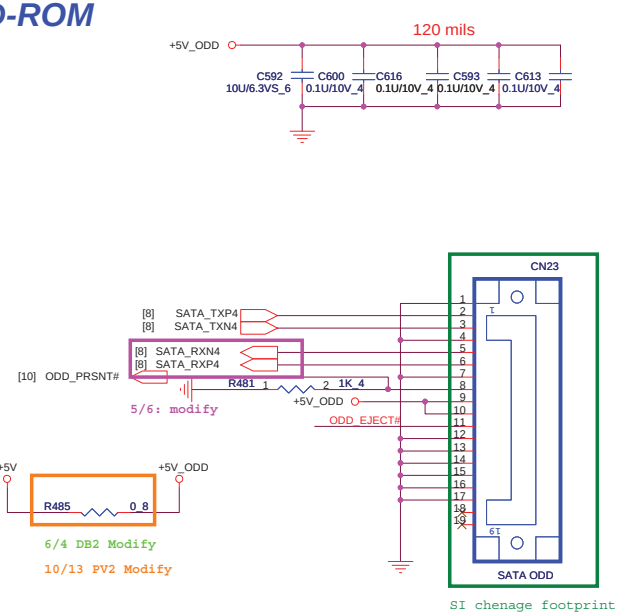
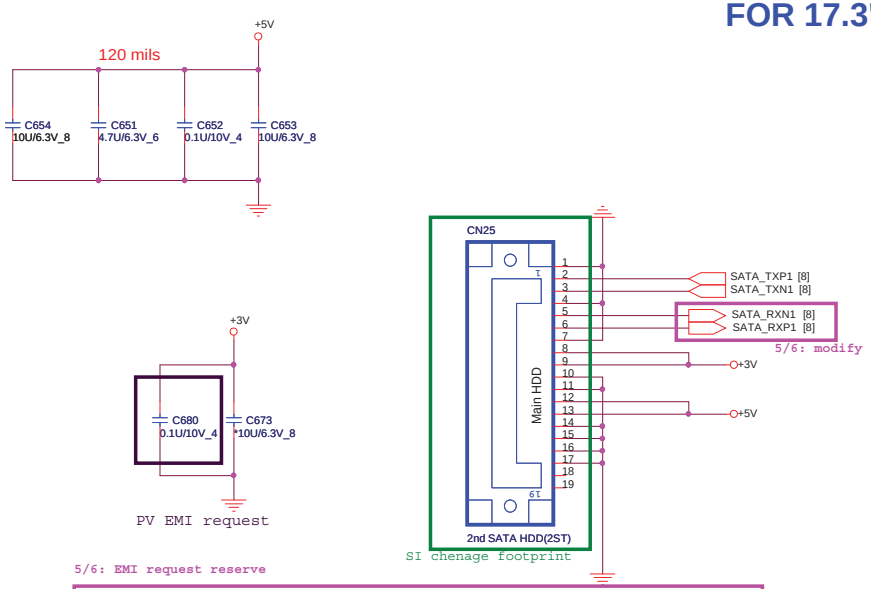
SATA HDD CONNECTOR

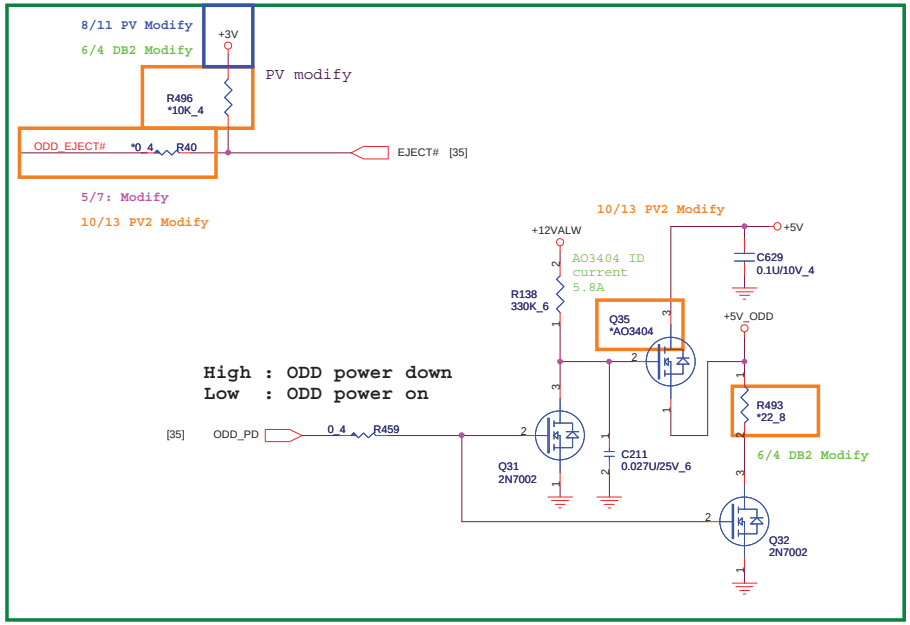


SATA CD-ROM



SATA_2 CONNECTOR FOR 17.3"





+3VPCU [7,8,25,32,35,36,37,38,39,40,42,44,45,47]
+1.05V [7,8,9,11,35,41]
+3V [3,7,8,9,10,11,13,14,18,19,25,26,27,28,29,30,31,32,33,35,36,37,39,40,41,43,45,46,47]
+5V [7,8,11,19,25,26,27,29,30,32,36,37,45]
+12VALW [25,37,42,44,45]

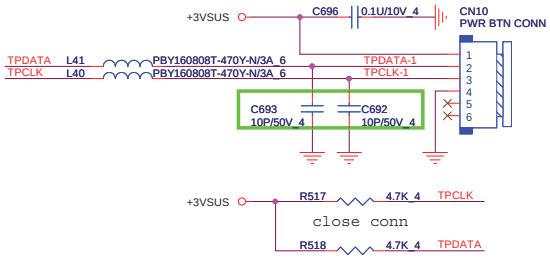
NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ODD/HDD/ANT	1A

Date: Wednesday, October 13, 2010 Sheet 34 of 47

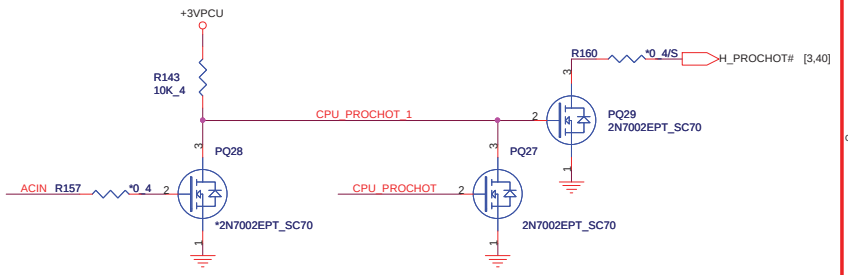
TOUCH PAD CONNECTOR & ON/OFF BOTTOM



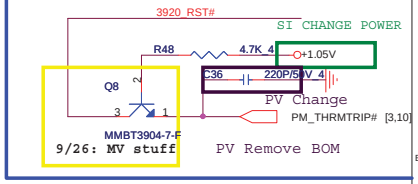
AC present: AC_IN-->high, CPU_PROCHOT-->low , H_PROCHOT#-->high

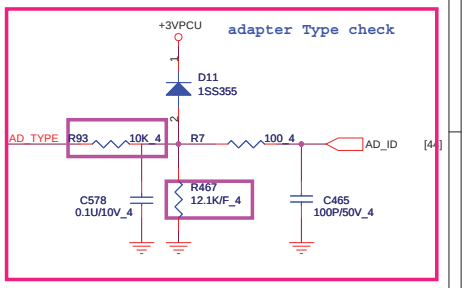
Remove AC: AC_IN-->low, CPU_PROCHOT-->low , H_PROCHOT#-->high

Remove AC and re-cove prochot: AC_IN-->low, CPU_PROCHOT--> high, H_PROCHOT#--> high

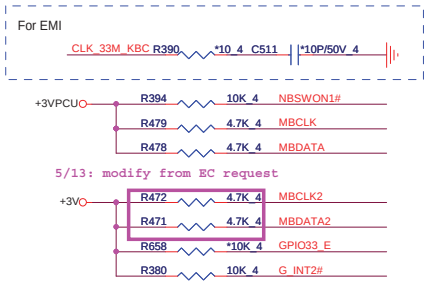


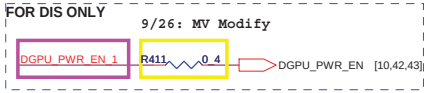
thermal shutdown circuit



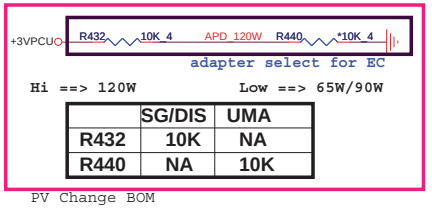


5/7 modify from power support 230w



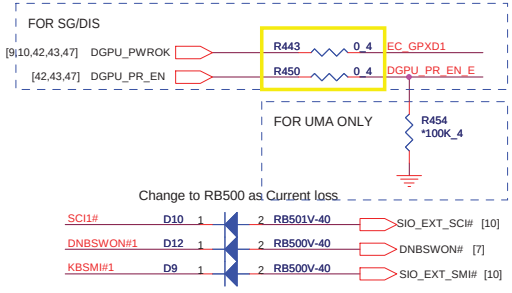


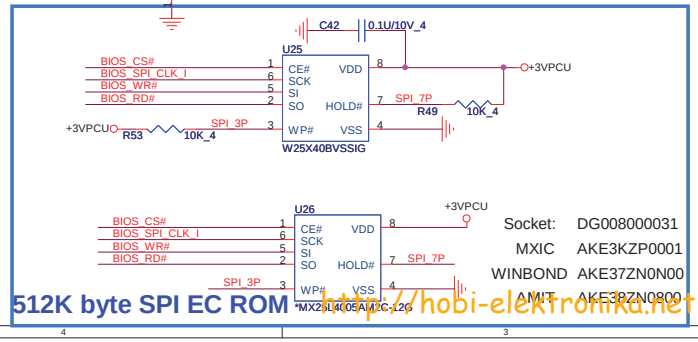
5/23: modify for stuff SG



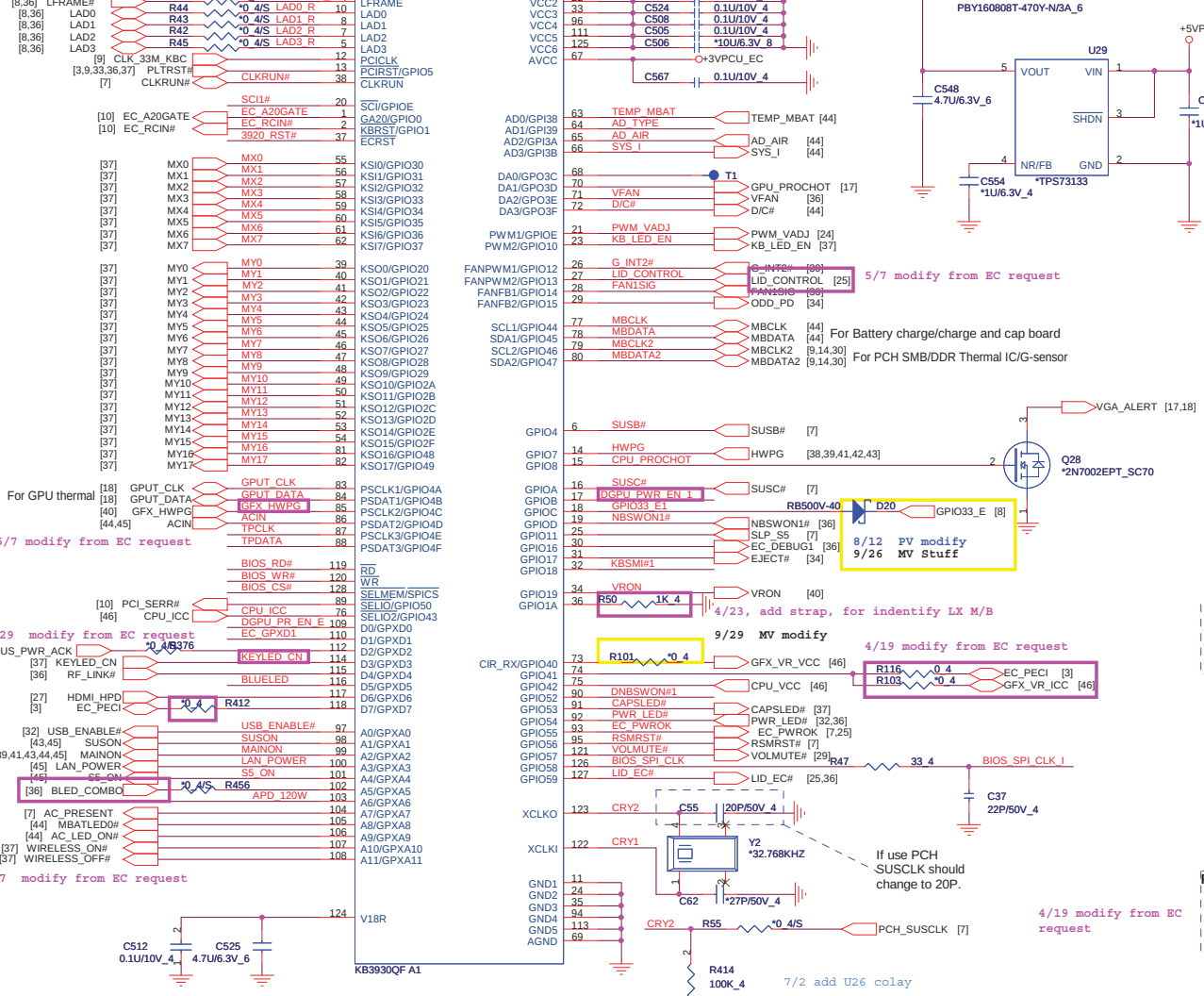
	SG/DIS	UMA
R432	10K	NA
R440	NA	10K

PV Change BOM





Socket:	DG008000031
MXIC	AKE3KZP0001
WINBOND	AKE37ZN0N00
ANT	AKE38ZN0B00



Project	PROJECT : LX3/5(Huron River)
Quanta	Quanta Computer Inc.
Size	Custom
Document Number	KB3926/ROM/TP
Rev	1A
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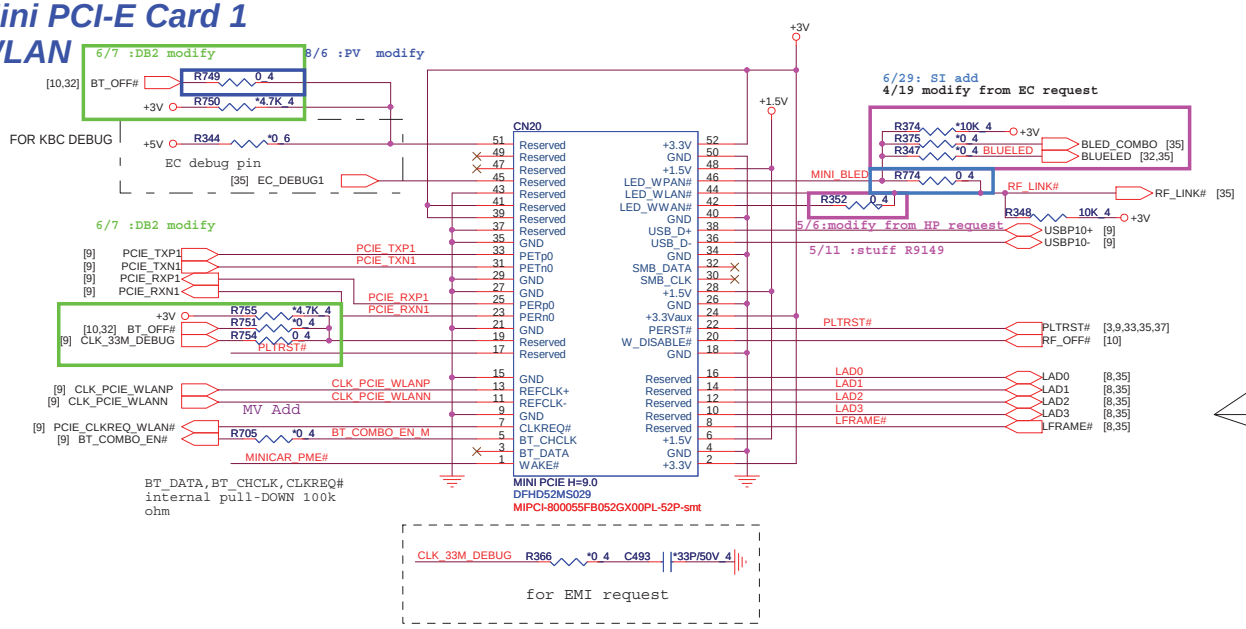
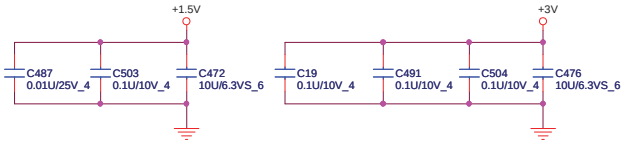
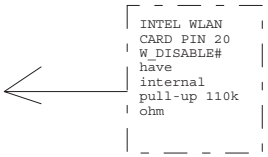
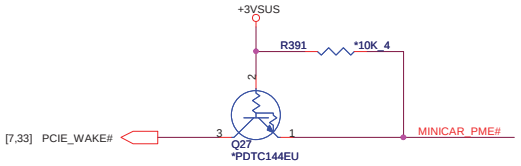
NB5

Mini PCI-E Card 1
WLAN



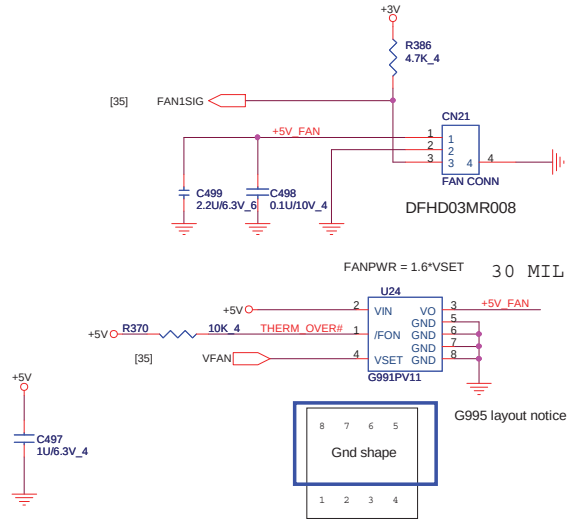




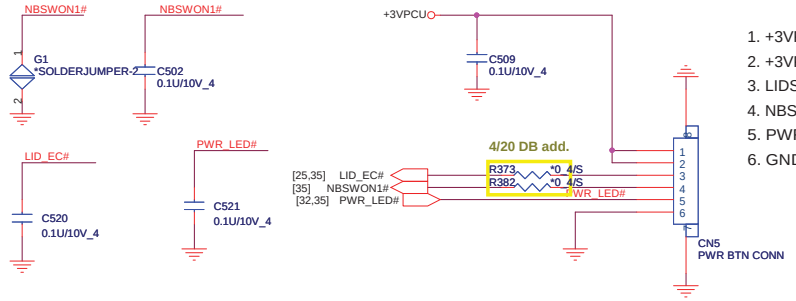


+3V [3,7,8,9,10,11,13,14,18,19,25,26,27,28,29,30,31,32,33,34,35,37,39,40,41,43,45,46,47]
+5V [7,8,11,19,25,26,27,29,30,32,34,37,45]
+1.5V [5,11,13,45]
+3VPCU [7,8,25,32,34,35,37,38,39,40,42,44,45,47]

CPU FAN



POWER BOTTON CONNECT



1. +3VPCU(LIDSWITCH PWR)
2. +3VPCU(LIDSWITCH PWR)
3. LIDSWITCH
4. NBSWON1#
5. PWRLED#
6. GND

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

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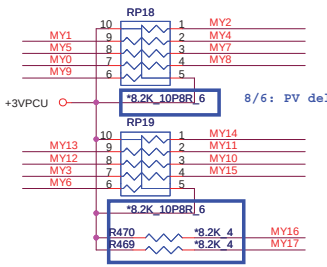
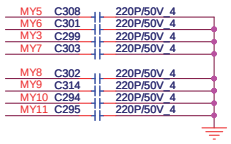
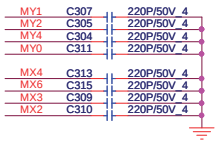
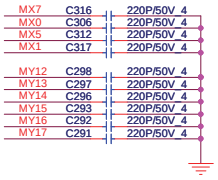
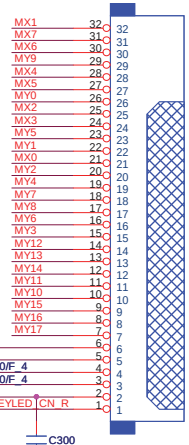
KEYBOARD PULL-UP



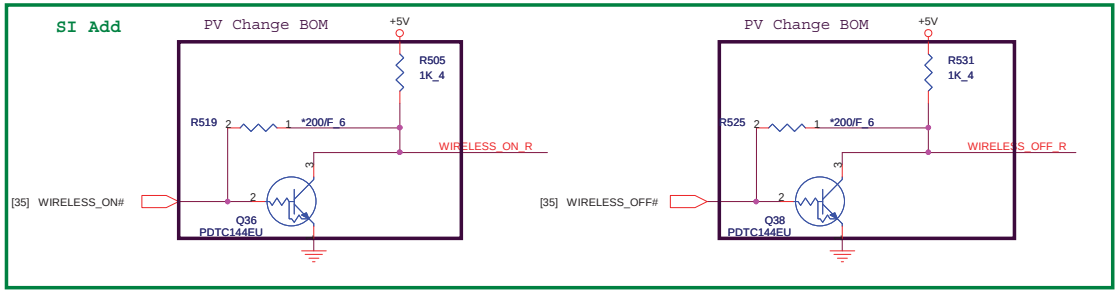


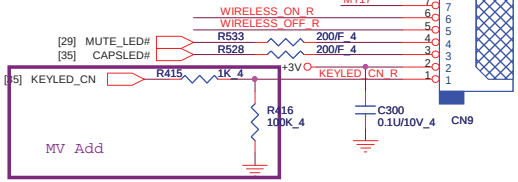


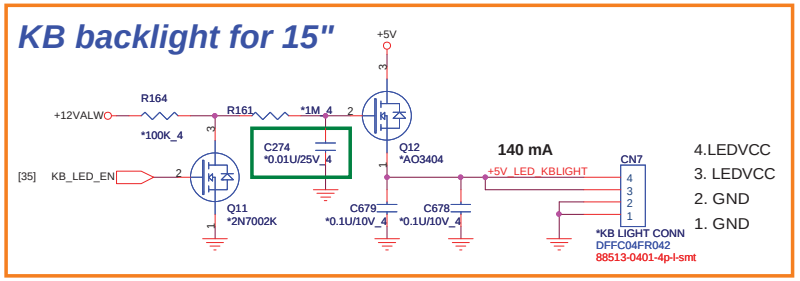


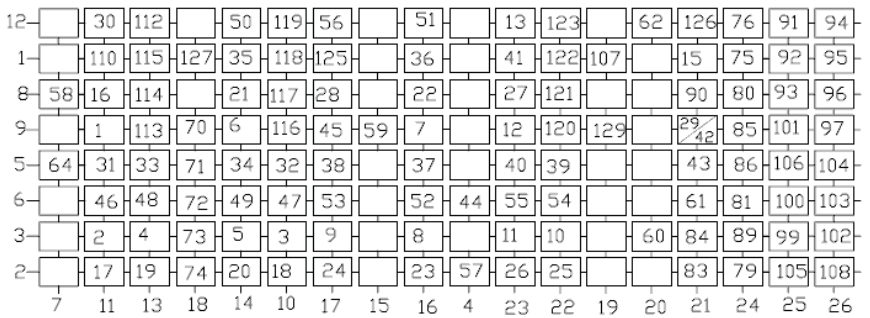


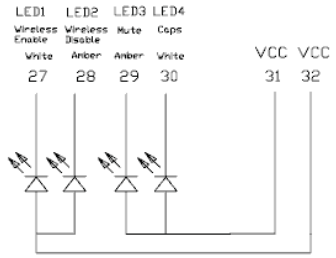
clear ABS 758 resin for key cap.
7 LEDs for 15.4" (total LED current 140mA)
11 LEDs for 17" (Total LED current 220mA)

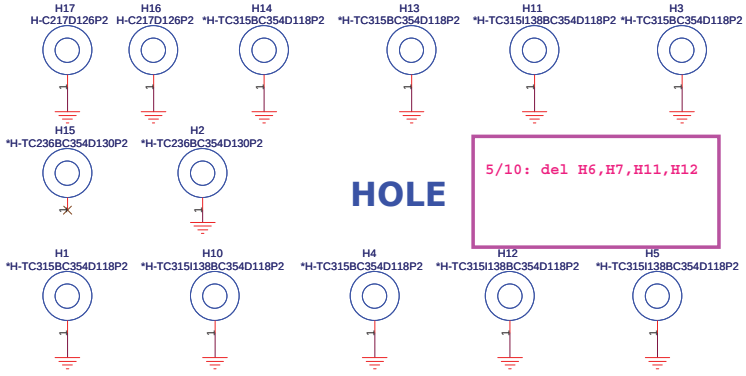






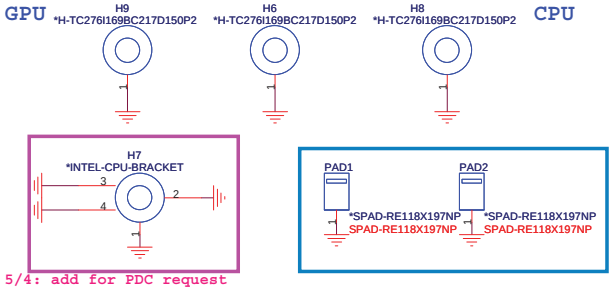




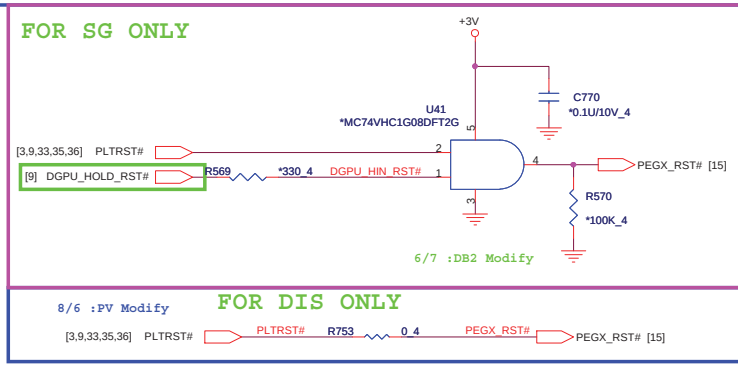


HOLE

5/10: del H6,H7,H11,H12



5/4: add for PDC request



+3V [3,7,8,9,10,11,13,14,18,19,25,26,27,28,29,30,31,32,33,34,35,36,39,40,41,43,45,46,47]
+5V [7,8,11,19,25,26,27,29,30,32,34,36,45]
+3VPCU [7,8,25,32,34,35,36,38,39,40,42,44,45,47]
+3V_VGA [16,17,18,19,27,42]
+12VALW [25,34,42,44,45]
+1.0V_VGA [15,17,19,43]
+1.5V_VGA [16,19,20,21,22,23,47]
+18V_VGA [15,17,19,21]

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

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DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

5VPCU setting			
	PR123		PQ16/PQ13
	Value	P/N	
35W CPU	133k	CS41332FB06	No POP
45W CPU	130k	CS41302FB00	POP

	PL13		PC38
	Value	P/N	
35W CPU	2.2uH	DC-22C0M000	No POP
45W CPU	1.5uH	DC-15G0M000	POP

+5V +/- 5% 35W/45W CPU
Countinue current:9A/12A
Peak current :12A/15A
OCP minimum :15A/20A

DB Change
Place these CAPs close to FETs
DB Change 35W CPU NA
PV change
Rds(on) 5m ohm
Rds(on) 14m ohm
NTC need place under CPU Socket
CPU Thermal protection at 90 +/-3 degrreC

+3.3V +/- 5%
Countinue current:6A
Peak current:7.5A
OCP minimum 9A

PU5 RT8206B

MAINON [35,39,41,43,44,45]
HWPG [35,39,41,42,43]
+VIN [25,31,39,41,42,43,44,45]
+3VPCU [7,8,25,32,34,35,36,37,39,40,42,44,45,47]
+5VPCU [32,35,39,40,41,42,43,44,45]

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Quanta Computer Inc.
NB5
Size Custom | Document Number +5V/+3V (RT8206B) | Rev 1A
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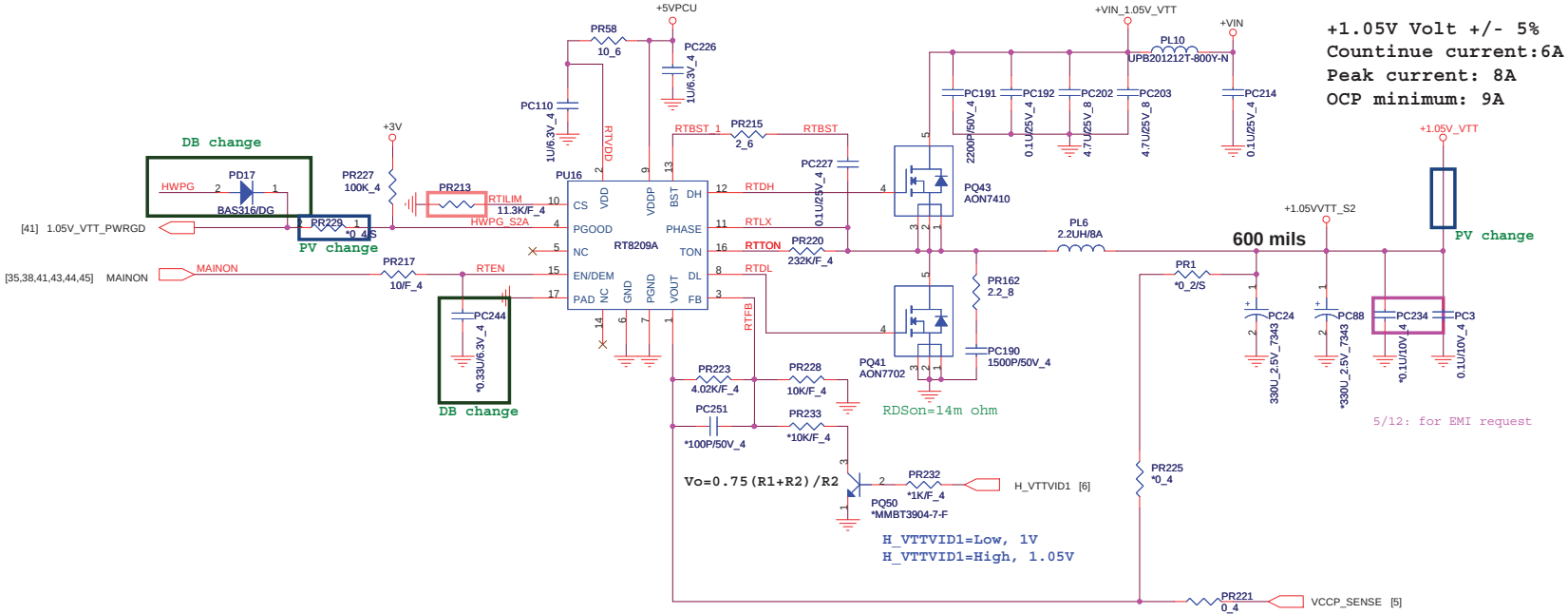

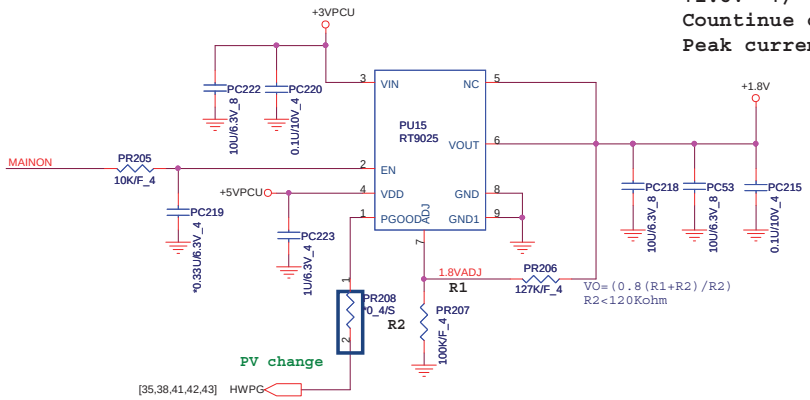

NB5	PROJECT : LX3/5(Huron River) Quanta Computer Inc.	
Size: Custom	Document Number: +1.05V/+1.8V (RT8204C)	Rev: 1A
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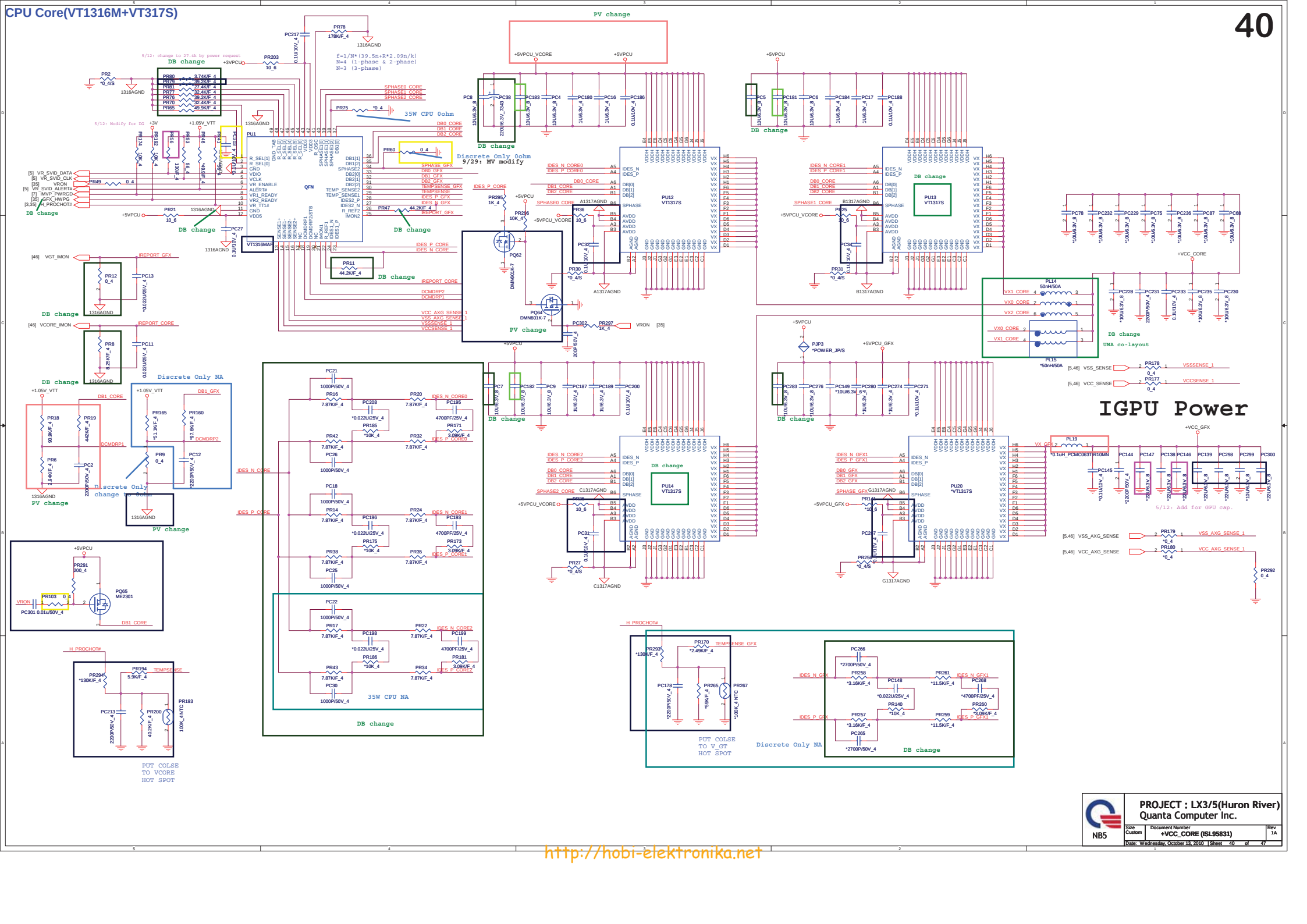

NB5	PROJECT : LX3/5(Huron River) Quanta Computer Inc.	
Size: Custom	Document Number: +VCC_CORE (ISL95831)	Rev: 1A
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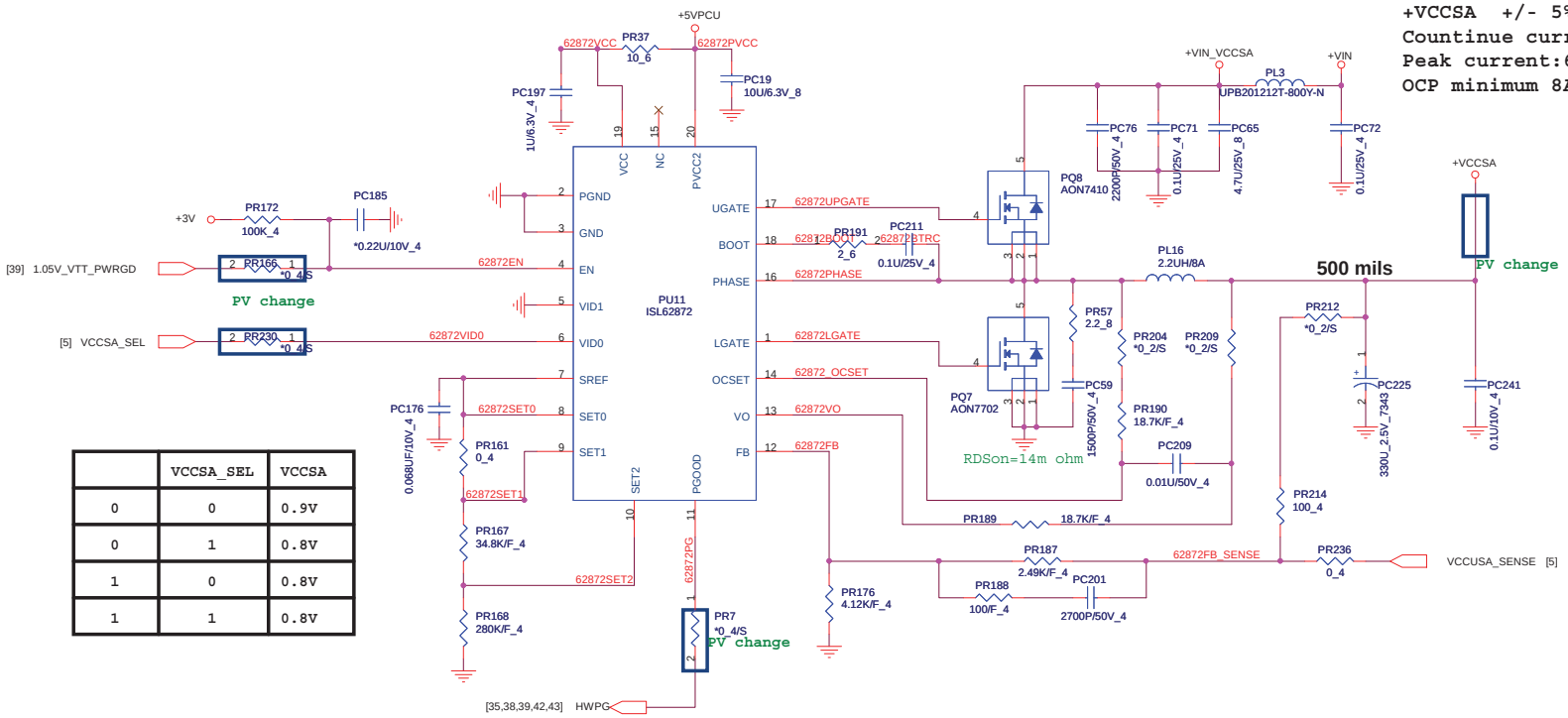
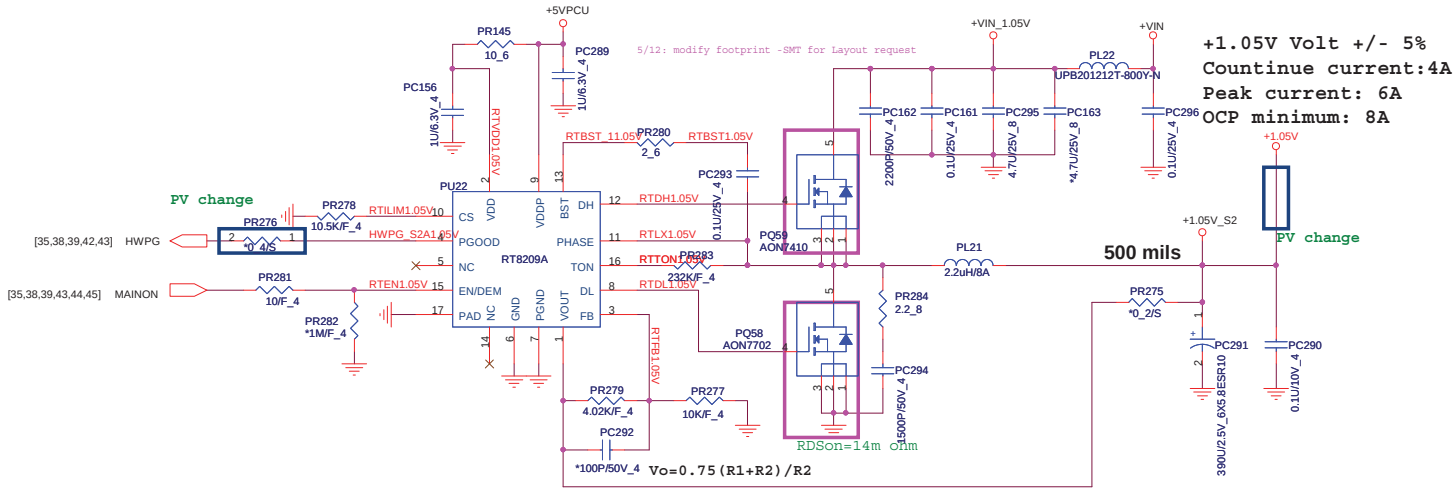
+VCCSA +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum 8A



	VCCSA_SEL	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.8V
1	1	0.8V

+1.05V Volt +/- 5%
Countinue current:4A
Peak current: 6A
OCP minimum: 8A



NB5

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.05V_VTT (VT358)	1A

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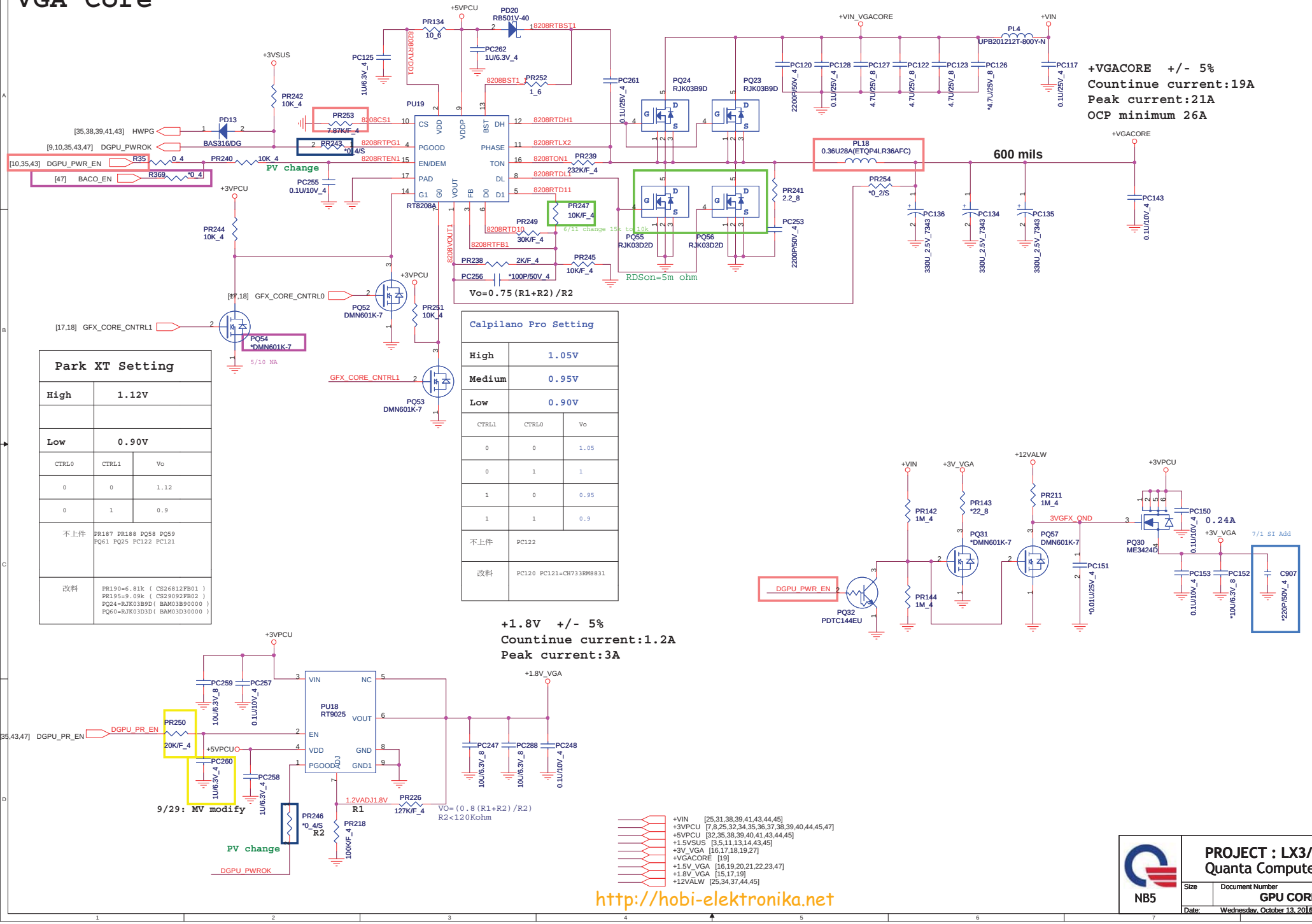
VGA Core



Park XT Setting		
High	1.12V	
Low	0.90V	
CTRL0	CTRL1	Vo
0	0	1.12
0	1	0.9
不上件	PR187 PR188 PQ58 PQ59 PQ61 PQ25 PC122 PC121	
改料	PR190=6.81k (CS26812FB01) PR195=9.09k (CS29092FB02) PQ24=RJK03B9D(BAM03B90000) PQ60=RJK03D3D(BAM03D30000)	

Calpilano Pro Setting		
High	1.05V	
Medium	0.95V	
Low	0.90V	
CTRL1	CTRL0	Vo
0	0	1.05
0	1	1
1	0	0.95
1	1	0.9
不上件	PC122	
改料	PC120 PC121=CH733RM8831	

+VIN [25,31,38,39,41,43,44,45]
+3VPCU [7,8,25,32,34,35,36,37,38,39,40,44,45,47]
+5VPCU [32,35,38,39,40,41,43,44,45]
+1.5VSUS [3,5,11,13,14,43,45]
+3V_VGA [16,17,18,19,27]
+VGACORE [19]
+1.5V_VGA [16,19,20,21,22,23,47]
+1.8V_VGA [15,17,19]
+12VALW [25,34,37,44,45]

NB5

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Quanta Computer Inc.

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	GPU CORE(ISL6264)	1A
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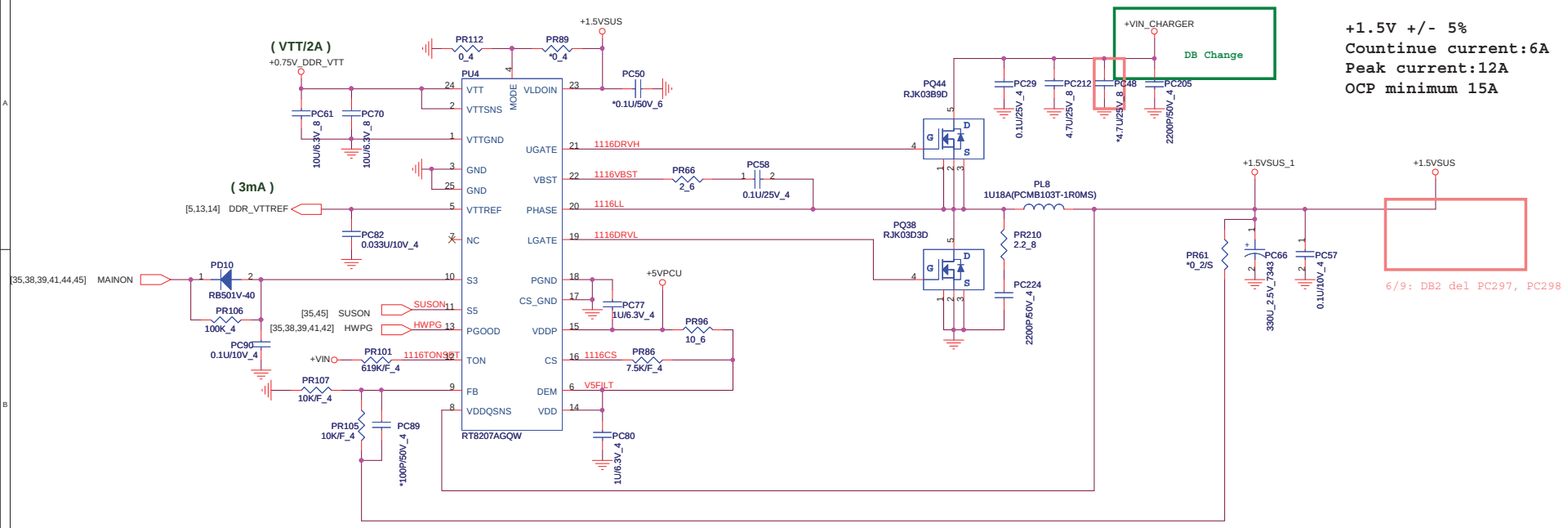
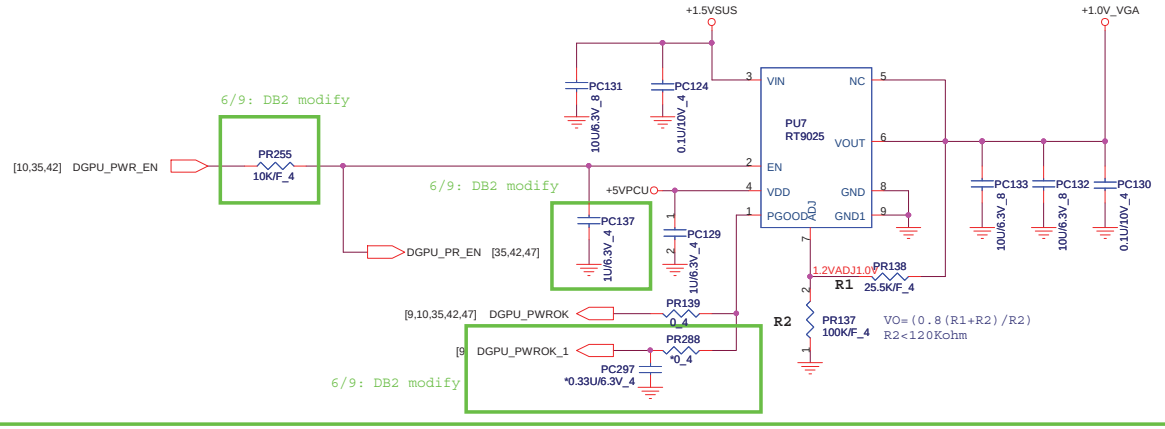
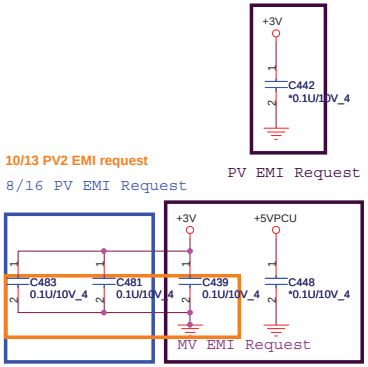


+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

SG & Discrete Only

+1.0V +/- 5%
Countinue current:1.7A
Peak current:3A





+3V [3,7,8,9,10,11,13,14,18,19,25,26,27,28,29,30,31,32,33,34,35,36,37,39,40,41,45,46,47]
+VIN [25,31,38,39,41,42,44,45]
+5VPCU [32,35,38,39,40,41,42,44,45]
+1.5VSUS [3,5,11,13,14,45]
+1.0V_VGA [15,17,19]
+0.75V_DDR_VTT [13,14,45]

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

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Custom	DDR3 (RT8207)	1A
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TOP DC_JACK
65W/90W

6/28: SI modify footprint

5/12: Mpdify footprint -SMT for layout request

6/30:SI Add

Do Not add test pad on BATDIS_G signal

PV change

15.6" DFHD08MR094
17.3" DFHD08MR096

CN18 DC-IN CONN

PU6 OZ8681

6/11: DB2 modify for power request

6/9: DB2 modify footprint

Place this cap close to EC

Place this cap close to EC

+VA [45]
+VH28 [45]
+VAD_1 [45]
+3VPCU [7,8,25,32,34,35,36,37,38,39,40,42,45,47]
+5VPCU [32,35,38,39,40,41,42,43,45]
+BATCHG [45]

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Charger (BQ24704)	1A

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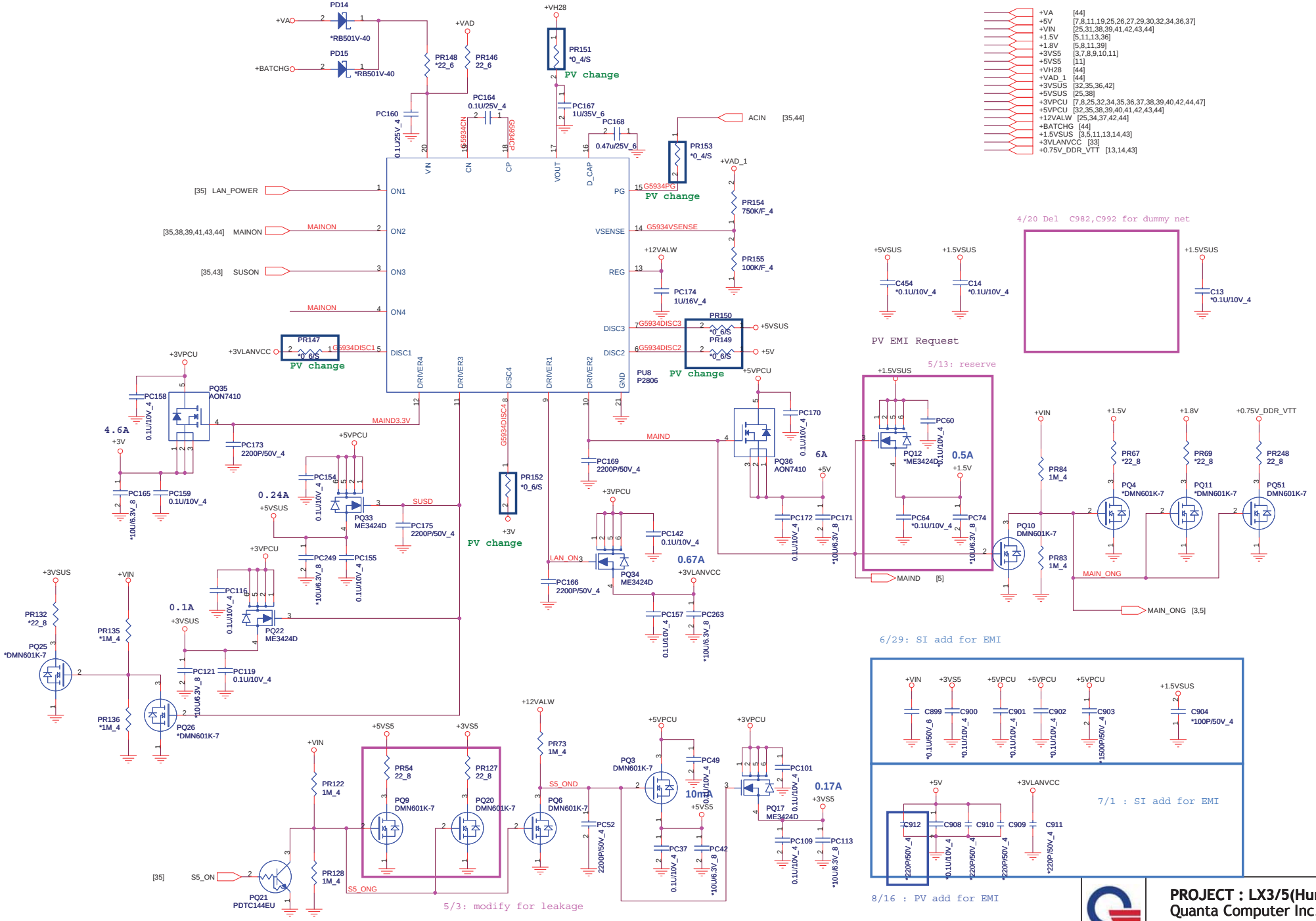

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Quanta Computer Inc.	
Size: Custom	Document Number: Dis-charge IC (P2806)
Rev:	1A
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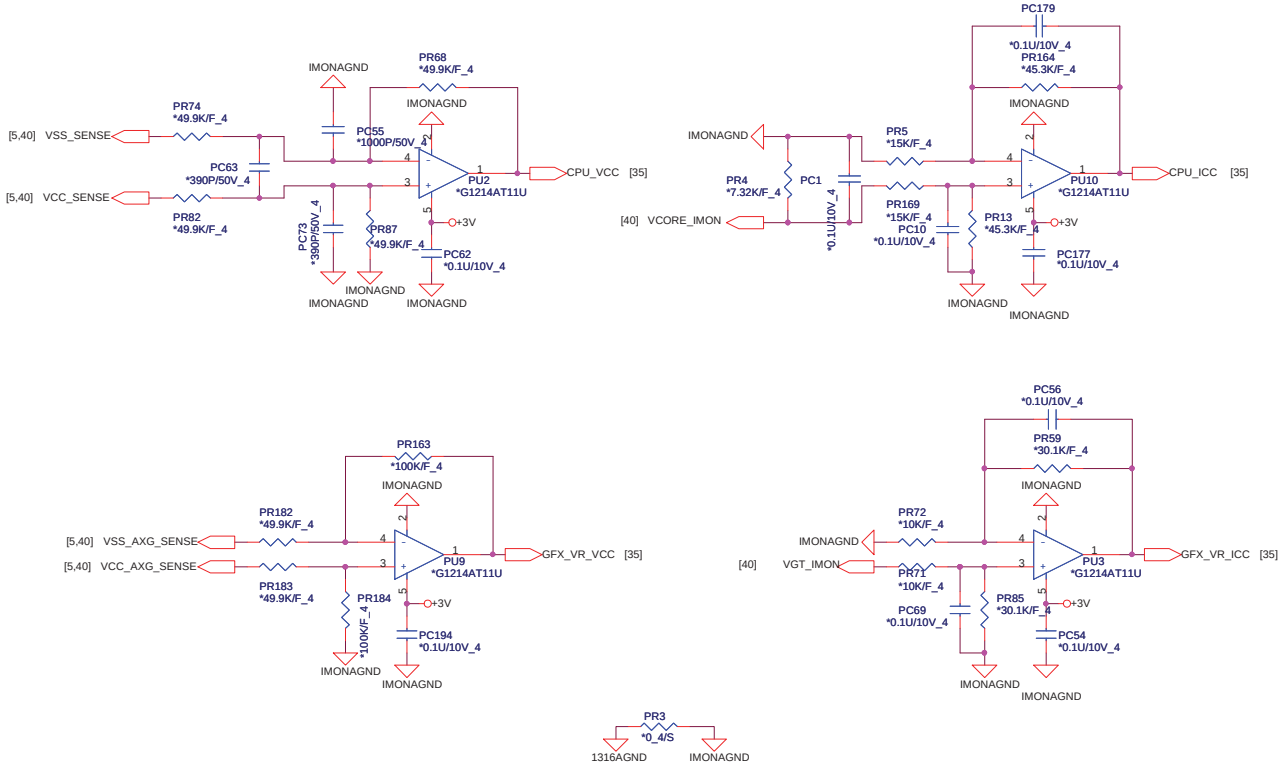

Vender	Size	P/N
EON	128KB	
	512KB	AKE37ZN0Q01 (EN25F40-100HIP)
Winbond	128KB	AKE35FN0N00 (W25X10BVSNIG)
	512KB	AKE37FN0N01 (W25X40BVSSIG)
Socket		DG008000031

NB5

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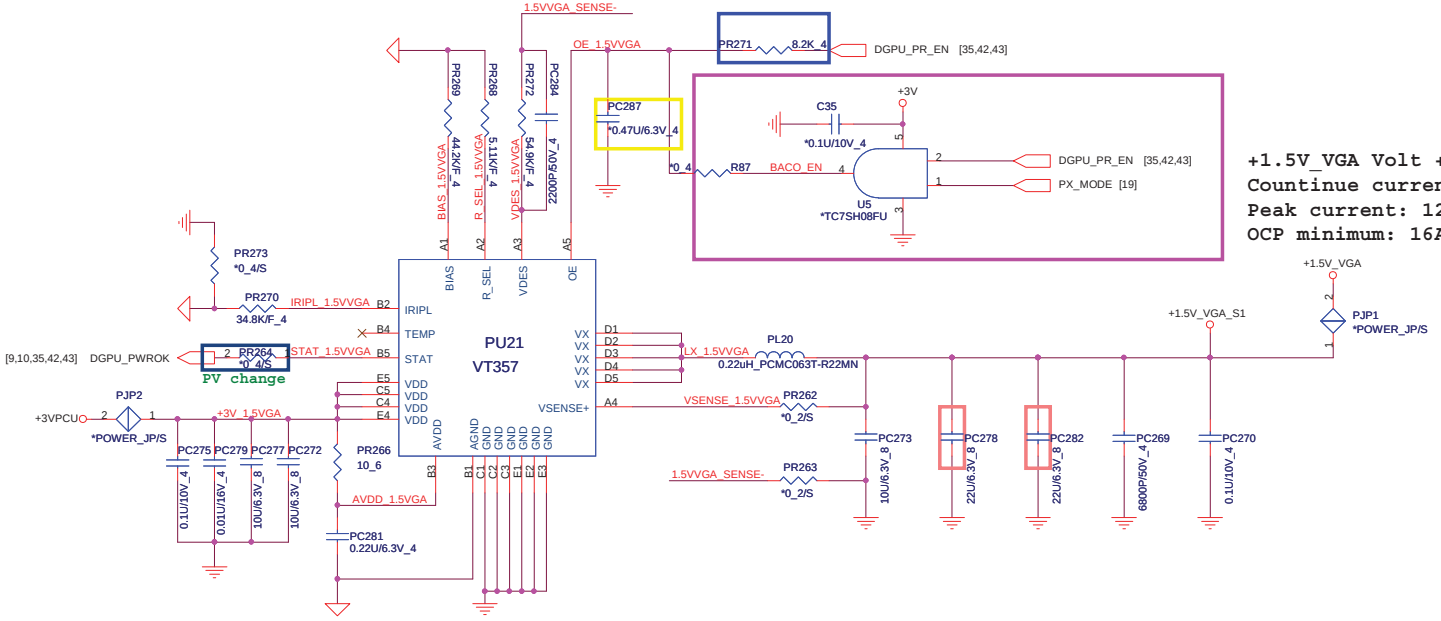
BACO_EN [42]
+1.5V_VGA [16,19,20,21,22,23]
+3VPCU [7,8,25,32,34,35,36,37,38,39,40,42,44,45]

9/29: MV modify



+1.5V_VGA Volt +/- 5%
Countinue current:8A
Peak current: 12A
OCP minimum: 16A

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

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Custom	+1.5V_VGA	1A
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